Silesian University of Technology
Faculty of Automatic Control, Electronics and Computer Science

Annual Review 2010

Institute of Electronics

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Edited by
Maria Drelichowska

Institute of Electronics, March 2011

FOREWORD

The Institute of Electronics is a part of the Faculty of Automatic Control, Electronics and Computer Science, one of the 12 faculties of the Silesian University of Technology, founded in 1945. The University is located in Gliwice and has about 28,000 students at present. The Faculty of Automatic Control was founded in 1964, and after a few reorganisations it changed its name to the Faculty of Automatic Control, Electronics and Computer Science. The total number of students is about 3,200 now. Since its creation in 1974 the Institute of Electronics has undergone a number of reorganisations. It has about 100 members of academic staff and consists of six divisions:

- ***Division of Electronics Fundamentals and Radio Engineering***
- ***Division of Digital and Microprocessor Systems***
- ***Division of Circuit and Signal Theory***
- ***Division of Telecommunication***
- ***Division of Biomedical Electronics***
- ***Division of Microelectronics and Biotechnology***

Last year the Biomedical Engineering Group was formed within the Division of Biomedical Electronics. In the academic year 2011/2012 its staff is expected to start teaching and research activities as the thirteenth faculty of the university, namely the Faculty of Biomedical Engineering.

The Institute specialises in such advanced fields of engineering as analogue and digital electronic systems, including biomedical systems, production of telecommunication and electronic systems etc. Research in these areas ranges from component to system level, encompassing practical and theoretical investigations with the application of both hardware and software techniques. Research groups are supported by a wide range of test and instrumentation equipment together with computer facilities, which can run with programming languages of all levels and offer various application software. Many of the Institute's research programmes are carried out in close co-operation with industry in order to satisfy the needs of the region, which is the main industrial centre of Poland.

The Institute offers 3.5-year courses leading to the degree of BSc in the general field of Electronics and Telecommunication and 1.5-year MSc courses in the following specialisations:

- Electronic Apparatus
- Biomedical Electronics
- Microelectronics
- Radio Engineering
- Telecommunication

Both degrees are obtained on the basis of a project and a report, presented during a final examination. Since 2007 two-stage courses in Biomedical Engineering have also been run. In addition, the Institute participates in a joint macro-course in Automatic Control, Electronics and Computer Science, run by the Faculty, in which all teaching is in the English language. The courses normally consist of lectures, laboratories, seminars and

projects, and are followed by examinations. Apart from this, the Institute offers four-year courses at evening studies, leading to the degree of BSc. The curricula of the courses run by the Institute are designed for people who want to achieve both theoretical knowledge and practical skills in electronics. Other didactic activities include postgraduate and PhD studies.

The following pages provide detailed information regarding the research carried out as well as the subjects taught in each division.

CONTENTS

DIRECTORS OF THE INSTITUTE

Director of the Institute:
Prof. Edward HRYNKIEWICZ

Vice Director of the Institute for Research:
Prof. Zdzisław FILUS

Vice Director of the Institute for Teaching:
Dr. Jacek KONOPACKI

DIVISION OF ELECTRONICS FUNDAMENTALS AND RADIO ENGINEERING

Head of Division: Prof. Zdzisław Filus, PhD, DSc

Research staff

Prof. Zdzisław FILUS, PhD, DSc

Prof. Andrzej KARWOWSKI, PhD, DSc
Prof. Leon LASEK, PhD, DSc
Asst. Prof. Adam BŁASZKOWSKI, PhD
Asst. Prof. Władysław CIĄŻYŃSKI, PhD
Andrzej BŁONAROWICZ, PhD
Jacek CHĘCIŃSKI, PhD
Jerzy FIOŁKA, PhD
Zenon KIDOŃ, PhD
Adam KRISTOF, PhD
Sławomir LASOTA, PhD
Mirosław MAGNUSKI, PhD
Andrzej MALCHER, PhD
Artur NOGA, PhD
Wojciech OLIWA, PhD
Zbigniew RYMARSKI, PhD
Maciej SURMA, PhD
Włodzimierz SZMELCER, PhD
Tomasz TOPA, PhD
Grzegorz WIECZOREK, PhD
Dariusz WÓJCIK, PhD

PhD Students

Adam POPOWICZ, MSc
Piotr FALKOWSKI, MSc

Research fields

- Electronic circuits synthesis
- Symbolic methods of electronic circuits analysis
- Electronic circuits for automotive applications
- Power electronic circuits
- Microprocessor-based measurement systems
- Computational electromagnetics
- Numerical modelling of radiating and scattering wire objects
- Linear antenna theory
- Electromagnetic compatibility
- Optoelectronics, Fiberoptics

Courses

- Semiconductor Devices
- Analogue Electronic Circuits
- Analogue Circuits Design
- Electronic Measurement Techniques
- Switching Circuits
- Special Semiconductor Devices and Circuits
- Materials Technology and Electronic Equipment Design
- Field and Wave Electromagnetics
- Introduction to Radiocommunication
- Radio Engineering Systems
- Fields, Waves and Antennas
- Wireless Computer Networks
- Design of Radio Electronic Devices
- High-Frequency Engineering Fundamentals
- Electromagnetic Compatibility

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

Head of Division: Prof. Edward Hrynkiewicz, PhD, DSc

Research staff

Prof. Edward HRYNKIEWICZ, PhD, DSc

Prof. Andrzej HŁAWICZKA, PhD, DSc
Asst. Prof. Zdzisław POGODA, PhD
Mirosław CHMIEL, PhD
Robert CZERWIŃSKI, PhD
Tomasz GARBOLINO, PhD
Krzysztof GUCWA, PhD
Józef KULISZ, PhD
Adam MILIK, PhD
Adam PAWLAK, PhD
Krzysztof PUCHER, PhD
Tomasz RUDNICKI, PhD
Wojciech SAKOWSKI, PhD
Dariusz STACHAŃCZYK, PhD
Krzysztof TABOREK, PhD
Bernard WYRWOŁ, PhD
Dariusz POLOK, MSc

PhD Students

Jan MOCHA, MSc
Danuta PAMUŁA, MSc
Jakub MURAWSKI, MSc
Paweł SZWARC, MSc

Research fields

- Testing and testability of digital systems
  - Generation of test patterns
  - I_{DDQ} testing
  - Design for testability
  - Built-in self-tests and concurrent testing
  - Pseudorandom techniques for built-in tests for VLSI circuits and design of standard P1149 compatible chips
  - Microcomputer signature analysis
- Design of systems with programmable devices and controllers
  - Design of support software
  - Logic synthesis
  - Technology mapping in CPLDs, FPGAs and PSoCs
  - Fast operating CPU structures of programmable controllers and methods of PLC programming
  - Distributed structures of PLCs

    - PLC applications
    - Embedded control system design
- Frequency multipliers based on digital techniques
- Laboratory and industrial data acquisition and control systems
    - Signal conditioning
    - Analogue-to-digital and digital-to-analogue converters with optical isolation and fibre optic transmission systems
- Multiprocessor systems
    - Pipelining and parallel processing
    - Systems with global memory and arbitration
    - Statistical analysis of performance for pipelining processing
- ASIC design
    - High level design methodologies
    - System modelling and simulation (using VHDL and Verilog)
    - IP-core design
    - Distributed design methodologies based on Internet

Courses

- Digital Systems Fundamentals
- Design of Digital Devices
- Microprocessors Fundamentals
- Microprocessor Systems
- Reliability and Testing of Electronic Devices
- Computer Aided Design of Integrated Circuits
- Programmable Logic Devices
- Programmable Controllers

DIVISION OF CIRCUIT AND SIGNAL THEORY

Head of Division: Prof. Jerzy Rutkowski, PhD, DSc

Research staff

Prof. Jerzy RUTKOWSKI, PhD, DSc

Jacek KONOPACKI, PhD, DSc
Tomasz GOLONEK, PhD
Tadeusz GRABOWIECKI, PhD
Damian GRZECHCA, PhD
Jan MACHNIEWSKI, PhD
Katarzyna MOŚCIŃSKA, PhD
Andrzej PUŁKA, PhD
Łukasz CHRUSZCZYK, PhD
Piotr JANTOS, PhD

PhD Students

Piotr KYZIOŁ, MSc

Research fields

- Computer-aided electronic circuits analysis and design
  - Failure diagnostics in analogue electronic circuits
  - Application of sensitivity methods to the analysis and synthesis of electronic circuits
  - Modelling and simulation of digital and mixed analog-digital circuits in VHDL language
  - System level design in SystemC
  - Application of artificial intelligence methods and genetic algorithms to circuit theory and electronics
  - Common-sense reasoning modelling and application of AI techniques to circuits models generation and verification
- Digital signal processing focused on digital filters design and application
- Signal processing and basic research into neural networks (analysis, synthesis and optimisation) and their application to engineering practice
  - Application of neural networks to image processing and recognition, including texture images
  - Application of wavelet techniques to signal processing
- Web – based education

Courses

- Circuit Theory
- Signal Theory
- Fundamentals of Electrical Engineering
- Information Theory and Coding
- Computer-Aided Design of Electronic Circuits
- Digital Signal Processing
- Biomedical Digital Signal Processing
- Neural Networks

DIVISION OF TELECOMMUNICATION

Head of Division: Dr. Jacek Izydorczyk

Research staff

Jacek IZYDORCZYK, PhD

Prof. Dariusz KANIA, PhD, DSc
Adam DUSTOR, PhD
Maria DZICZKOWSKA, PhD
Leszek DZICZKOWSKI, PhD
Grzegorz DZIWOKI, PhD
Piotr KŁOSOWSKI, PhD
Marcin KUCHARCZYK, PhD
Andrzej KUKIEŁKA, PhD
Wojciech SUŁEK, PhD
Jerzy WOJTUSZEK, PhD
Piotr ZAWADZKI, PhD

Research fields

- Digital commutation in modern telecommunication systems
  - Construction of telephone exchanges
  - Supervisory software for telephone exchanges
  - Special services (e.g. teleconferences)
  - Implementation of digital networks with integrated services (ISDN, B-ISDN, ATM)
- Application of digital signal processing to telecommunication
  - Compression of speech signal with the application of DSPs
  - Speech synthesis
  - Speech and speaker recognition
  - Application of artificial neural networks to signal processing
  - Design, testing and implementation of error correcting and modulating codes
  - Design of modern local area networks
  - Implementation and testing of new services in the Internet
  - xDSL technology
  - Efficient hardware implementation of decoder of LDPC code.

- Electromagnetic field engineering
  - Radiation and scattering of electromagnetic waves
  - Lightning protection
- Modems

Courses

- Fundamentals of Analogue and Digital Communication
- Fundamentals of Commutation
- Switching Nodes and Exchanges
- Principles of Transmission
- Communication Systems
- Signal Theory
- Information Theory and Coding
- Digital Signal Processing
- Computer-Aided Analysis of Electronic Circuits
- Digital Signal Processors (DSP)
- Neural Networks
- Computer Networks
- Internet
- Modems
- Introduction to Cryptography

DIVISION OF BIOMEDICAL ELECTRONICS

Head of Division: Prof. Jacek Łęski, PhD, DSc

Research staff

Prof. Jacek ŁĘSKI, PhD, DSc

Prof. Ewa PIĘTKA, PhD, DSc
Paweł BADURA, PhD
Robert CZABAŃSKI, PhD
Norbert HENZEL, PhD
Jerzy IHNATOWICZ, PhD
Jacek KAWA, PhD
Marian KOTAS, PhD
Tomasz PANDER, PhD
Stanisław PIETRASZEK, PhD
Sylwia POŚPIECH-KURKOWSKA, PhD
Tomasz PRZYBYŁA, PhD
Dominik SPINCZYK, PhD
Ewa STRASZECKA, PhD
Wojciech WIĘCŁAWEK, PhD
Piotr ZARYCHTA, PhD

PhD Students

Monika BUGDOL, MSc
Michał JEŻEWSKI, MSc
Jan JUSZCZYK, MSc
Joanna CZAJKOWSKA, MSc
Marcin RUDZKI, MSc
Przemysław SZABELAK, MSc

Research fields

- Biocybernetics and biomedical engineering - processing of information in medicine
  - Processing of biomedical signals
  - Image processing and analysis
  - Fuzzy sets and systems, neuro-fuzzy systems
  - Pattern recognition
  - Cybernetics
  - Computer assisted medical diagnosis
  - Image guided surgery
  - Hospital information system
  - Picture archiving and communications systems
  - Medical information systems integration
  - Expert systems in medicine
  - Time-frequency analysis of biomedical signals

    - Multirate signal processing
    - Evolutionary computations
    - Artificial neural networks
    - Data mining
    - Artificial intelligence

- Design, construction and testing of electronic medical apparatus
    - Design and construction of amplifiers for biological signals and data acquisition systems co-operating with computers
    - Testing of electromedical apparatus
    - Design of electronic devices for data acquisition

Courses

- Electromedical Metrology
- X-ray and Nuclear Imaging
- Medical Information Systems
- Cybernetics
- Electromedical Equipment
- Pattern Recognition
- Principles of Knowledge Engineering
- Diagnostic Imaging Systems
- Biocybernetics
- Computers in Medicine
- Diagnostic Cardiological Systems
- Computer Aided Medical Diagnosis
- Materials Science and Principles of Construction of Electronic Equipment
- Probability Theory and Mathematical Statistics
- Numerical Methods
- Biomedical Information Processing

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

Head of Division: Prof. Jacek Szuber, PhD, DSc

Research staff

Prof. Jacek SZUBER, PhD, DSc

Prof. Ewaryst TKACZ, PhD, DSc
Asst. Prof. Zbigniew PRUSZOWSKI, PhD
Wojciech FILIPOWSKI, PhD
Weronika IZYDORCZYK, PhD
Dariusz KOMOROWSKI, PhD
Paweł KOSTKA, PhD
Piotr KOWALIK, PhD
Monika KWOKA, PhD
Jerzy ULJANOW, PhD
Krzysztof WACZYŃSKI, PhD
Edyta WRÓBEL, PhD

PhD Students

Artur GINTROWSKI, MSc
Michał SITARZ, MSc

Research fields

- Biotechnology and bioinformatics
  - Analysis of gene expressions
  - Computer assisted medical diagnosis
  - Time-frequency analysis of biomedical signals
  - Multirate signal processing
  - Evolutionary computations
- Design of electronic devices for data acquisition
- Technology of doped semiconductor glasses based on organosilicon compounds
- Special hybrid circuits made in thick (thin) film technology
- Solar cells and photovoltaic systems
- Passivation of semiconductor surfaces for application in microelectronics
- Nanotechnology of transparent conductive oxides and organic semiconductors for application in photovoltaics and gas sensorics

Courses

- Materials Science and Principles of Construction of Electronic Equipment
- Electromedical Metrology
- Bionics
- Computers in Medicine
- Biotechnology in Medicine
- Computer Assisted Diagnostics in Medical Care
- Artificial Organs
- Physics in Medicine
- Physics
- Solid-State Physics
- Physics of Microfabrication
- Principles of Electron Technology
- Microelectronics
- Electronic Devices, Semiconductor Structures and Circuits
- Sensors and Actuators
- Semiconductor Devices
- Thick-Film Technology
- Design of Thick/Thin-Film Circuits
- Hybrid Circuit Technology
- Hermetic Sealing
- Thin-Film Technology
- Nanotechnology in Microelectronics

STATUTORY ACTIVITIES OF THE INSTITUTE OF ELECTRONICS

DSc DEGREES CONFERRED ON STAFF MEMBERS OF THE INSTITUTE OF ELECTRONICS

1. **Konopacki J.** – DSc examination on the basis of the monograph entitled "Design of infinite impulse response digital filters (IIR) – selected problems" took place at the Faculty of Automatic Control, Electronics and Computer Science, Silesian University of Technology, on 9 November 2010.
2. **Rymarski Z.** – DSc examination on the basis of the monograph entitled "Single-phase and three-phase voltage source inverters for UPS systems" took place at the Faculty of Automatic Control, Electronics and Computer Science, Silesian University of Technology, on 30 November 2010.

PhD DEGREES CONFERRED ON STAFF MEMBERS AND PhD STUDENTS OF THE INSTITUTE OF ELECTRONICS

1. **Rafał Doniec**, Application of Artificial Intelligence Methods for Human Organism Insulin Level Regulation, PhD advisor: Prof. Ewaryst Tkacz, 25 October 2010

RESEARCH GRANTS

Research activities of the Institute of Electronics are mainly financed by the Ministry of Science and Higher Education within the frames of a general research programme:

- ***Development of new research areas in electronics, telecommunication and signal processing***

Apart from this, each division of the Institute carries out its own research in the following general areas, which are further subdivided into individual research projects:

Division of Electronics Fundamentals and Radio Engineering:

- *Electronic components, circuits and systems - development of measurement methods, analysis and synthesis*

Division of Digital and Microprocessor Systems:

- *Multiprocessor systems, application specific integrated circuits programmable logic devices and systems - analysis, design and testing*

Division of Circuit and Signal Theory:

- *Computer-aided methods of analysis, synthesis and testing of electronic systems and their selected applications*

Division of Telecommunication:

- *Development of methods and applications of digital channel commutation and transmission of digital signals, theoretical and experimental methods of examination of bodies radiating and dissipating electromagnetic waves*

Division of Biomedical Electronics:

- *Acquisition and processing of biomedical information*

Division of Microelectronics and Biotechnology:

- *Application methods of microelectronic technologies and biotechnologies*

In total, fifty three individual research projects were completed in 2010.

GRANTS AWARDED BY THE COMMISSION OF EUROPEAN COMMUNITIES

VII Framework Programme of European Union

Structural Project – Operational Programme of Innovative Economy

Innovation Technology of Multifunctional Materials and Structures for Nanoelectronics, Photonics, Spintronics and Sensoric Techniques (InTechFun), Period: 2009-2013, Role in project: Prof. J. Szuber - Head of the group PSl-2

The project deals with the development of a new innovative technology of multifunctional materials and structures for nanoelectronics, photonics, spintronics and sensoric techniques. It has a form of a national network with the contribution of 6 Polish partners from academia and industry. The Institute of Electronics is responsible for 5 Workpackages dealing with technology and characterization of novel materials, structures and prototypes. Moreover, one Workpackage is devoted to the modernization of experimental systems for nanotechnological application. The project started on May 2009 and within this year the general organizational scheme for research and development was developed together with the implementation of experimental systems for future studies. In 2010 several scientific were realized within the new materials and new technological modules, together with the development of infrastructures for new materials characterization.

INDIVIDUAL RESEARCH GRANTS AWARDED BY THE MINISTRY OF SCIENCE AND HIGHER EDUCATION TO STAFF MEMBERS OF THE INSTITUTE

1. **Prof. E. Tkacz**, Elaboration of the New Methodology for Electrogastrographic Signals Examination Concerning Identification of Human Multi-channel EGG Characteristic Parameters Repeatability (duration: 16.10.2007 – 15.04.2010)
2. **Prof. E. Piętka**, Photodynamic image archiving, analysis and communication system in cancer diseases (duration: 1.05.2008 – 31.05.2011)
3. **Prof. A. Karwowski**, Fast hybrid methods of computational electromagnetics, (duration: 18.05.2008 - 18.05.2011)
4. **Prof. A. Karwowski**, Antennas for modern wireless systems for information society technologies - new structures, models, and methods of analysis and design (2009-2011)
5. **Dr T. Rudnicki**, Control algorithms for mechatronic systems of mechanical vehicles) (duration: 18.03.2010 – 17.03.2013)
6. **Prof. E. Hrynkiewicz, Dr A. Milik**, Fast reconfigurable logic controllers (duration: 13.04.2010 – 12.04.2012)
7. **P. Kyziol, MSc**, (PhD grant, advisor: Prof. J. Rutkowski), Testing analog electronic circuits using multidimensional search space and swarm intelligence algorithms
8. **Dr D. Grzechca**, (DSc grant), Modern testing and diagnosis methods for analog electronic circuits (duration: 21.04.2010 – 31.12.2010)

INTERNATIONAL CO-OPERATION

1. Technical University of Ostrava, Department of Measurements and Control, Czech Republic (Prof. E. Hrynkiewicz)
2. University of Southern California (Prof. E. Piętka)
3. SECTRA – Sweden (Prof. E. Piętka)
4. Chemnitz University of Technology, Germany (Prof. J. Szuber)
5. University of Tübingen, Germany, (Prof. J. Szuber)
6. Ecole Centrale de Lyon, Ecully, France, (Prof. J. Szuber)
7. University Clermont-Ferrand, France, (Prof. J. Szuber)

8. University of L'Aquila, Coppito, Italy, (Prof. J. Szuber)
9. Graz University of Technology, Austria, (Prof. J. Szuber)
10. Hokkaido University, Sapporo, Japan, (Prof. J. Szuber)
11. Kyushu University, Fukuoka, Japan, (Prof. J. Szuber)
12. Technical University of Prague, Institute of Bioengineering, Czech Republic (Prof. E. Tkacz)
13. Technical University of Stuttgart, Institute of Bioengineering, Germany (Prof. E. Tkacz)
14. California University, Department of Electrical Engineering and Computer Science, Berkeley, USA (Dr. A. Pułka)
15. Université Henri Poincaré, Nancy, France (Dr. N. Henzel)

SCIENTIFIC CONFERENCES ORGANISED AND CO-ORGANISED BY THE INSTITUTE OF ELECTRONICS

1. 2nd International Conference Information Technologies in Biomedicine, IEEE, Kamień Śląski, 7-9 June 2010 (Prof. E. Piętka)
2. International Conference on Signals and Electronic Systems, ICSES'10, IEEE Poland Section, Gliwice, 7-10 September 2010 (Prof. J. Rutkowski, Dr A. Pułka)
3. VII International Workshop on Semiconductor Gas Senors – SGS2010, Kraków, 12-16 September 2010 (Prof. J. Szuber)
4. X IFAC Workshop Programmable Devices and Embedded Systems (PDeS'10), Pszczyna, Poland, 6 – 7 October 2010 (Prof. E. Hrynkiewicz, Dr A. Milik)
5. The 8th International PhD Students' Workshop Control and Information Technology, Brno University of Technology, Brno, Czech Republic, 8 September 2010, (co-organization – Prof. Z. Filus)

STAFF MEMBERS PARTICIPATING IN SCIENTIFIC AND ORGANISING COMMITTEES OF CONFERENCES AND SYMPOSIA

International

1. **Dr T. Garbolino**, Steering Committee and Program Committee, 13th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2010, 14-16 April 2010, Vienna, Austria

2. **Dr K. Gucwa**, Program Committee, 13th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2010, 14-16 April 2010, Vienna, Austria
3. **Prof. A. Hławiczka**, Program Committee, 13th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2010, 14-16 April 2010, Vienna, Austria
4. **Prof. E.Hrynkiewicz**, Steering Committee and Program Committee, 13th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2010, 14-16 April 2010, Vienna, Austria
5. **Prof. E. Hrynkiewicz**, X Programmable Devices and Embedded Systems (PDeS'10) IFAC Workshop, Pszczyna, Poland, 6-8 October 2010
6. **Prof. E. Hrynkiewicz**, International Conference on Signals and Electronic Systems, ICSES'10, IEEE Poland Section, Gliwice, 7-10 September 2010
7. **Prof. E. Hrynkiewicz**, 34th International Microelectronics and Packaging IMAPS-CPMT Poland Conference, and 10th Conference "Electron Technology" ELTE 2010, Wrocław, 22-25 September 2010
8. **Dr. J. Izydorczyk**, Poland Section Chapter Chair, coordinator of the IEEE technical cosponsoring, The International Science Conference: Computer Networks - CN`10, 15-19 June 2010, Ustroń
9. **Prof. D. Kania**, X Programmable Devices and Embedded Systems (PDeS'10) IFAC Workshop, Pszczyna, Poland, 6-8 October 2010
10. **Prof. A. Karwowski**, Local Organizing Committee, EMC Europe 2010, EMC Europe 2010 9th International Symposium on EMC joint with 20th International Wroclaw Symposium on EMC, 13-17 September 2010, Wrocław, Poland
11. **Dr. A. Pawlak**, Steering Committee and Program Committee, 13th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2010, 14-16 April 2010, Vienna, Austria
12. **Prof. E. Piętka**, Chairwoman, 2nd International Conference Information Technologies in Biomedicine, IEEE, Kamień Śląski, 7-9 June 2010
13. **Dr. A. Pułka**, Co-chairman, International Conference on Signals and Electronic Systems, ICSES'10, IEEE Poland Section, Gliwice 7-10 September 2010

14. **Prof. J. Rutkowski**, Chairman, International Conference on Signals and Electronic Systems, ICSES'10, IEEE Poland Section, Gliwice 7-10 September 2010
15. **Prof. J. Rutkowski**, The International Science Conference: Computer Networks - CN`10, 15-19 June 2010, Ustroń
16. **Prof. J. Szuber**, Chairman, VII International Workshop on Semiconductor Gas Senors – SGS2010, Kraków, 12-16 September 2010
17. **Prof. J. Szuber**, 34th International Microelectronics and Packaging IMAPS-CPMT Poland Conference and 10th Conference "Electron Technology" ELTE 2010, Wrocław, 22-25 September 2010
18. **Prof. J. Szuber**, VII International Symposium on Solid State Surface and Interfaces, Smolenice (Slovakia), 22-26 November 2010
19. **Prof. E. Tkacz**, 2nd International Conference Information Technologies in Biomedicine, IEEE, Kamień Śląski, 7-9 June 2010
20. **Dr K. Waczyński**, 34th International Microelectronics and Packaging IMAPS-CPMT Poland Conference and 10th Conference "Electron Technology" ELTE 2010, Wrocław, 22-25 September 2010

National

1. **Prof. Z. Filus,** 9th National Electronics Conference, 30 May-2 June 2010, Darłówko Wschodnie
2. **Prof. E. Hrynkiewicz**, 9th National Electronics Conference, 30 May-2 June 2010, Darłówko Wschodnie
3. **Prof. E. Hrynkiewicz**, 12th National Conference Reprogrammable Digital Circuits, RUC 2010, 27-28 May 2010, Szczecin
4. **Prof. E. Hrynkiewicz**, Scientific Conference „Informatics – Art. Or Craft?" and Training Workshop of the Institute of Computer Science and Electronics of the Zielona Góra University, 7-11 June 2010
5. **Prof. D. Kania**, 12th National Conference Reprogrammable Digital Circuits, RUC 2010, 27-28 May 2010, Szczecin
6. **Prof. D. Kania**, Scientific Conference „Informatics – Art. Or Craft?" and Training Workshop of the Institute of Computer Science and Electronics of the Zielona Góra University, 7-11 June 2010
7. **Prof. L. Lasek**, 9th National Electronics Conference, 30 May-2 June 2010, Darłówko Wschodnie

8. **Prof. E. Piętka**, Conference Databases – Applications and Systems, 15-19 May 2010, Ustroń
9. **Prof. J. Rutkowski,** 9th National Electronics Conference, 30 May-2 June 2010, Darłówko Wschodnie
10. **Prof. J. Rutkowski**, Conference Databases – Applications and Systems, 15-19 May 2010, Ustroń
11. **Prof. J. Szuber**, 4th National Conference on Nanotechnology - NANO 2010, 28 June –4 July 2010, Poznań
12. **Prof. J. Szuber**, 9th Conference on Optical and Electronic Sensors COE2010, Nałęczów, 20-23 June 2010

REVIEWERS

1. **Dr. R. Czabański**, International Journal of Applied Mathematics and Computer Science
2. **Prof. Z. Filus**, International Journal of Electronics, national project proposals (Ministry of Science and Higher Education)
3. **Dr. T. Garbolino,** reviewer of EU project proposals
4. **Dr T. Golonek**, IEEE Transactions on Circuits and Systems II
5. **Dr. D. Grzechca**, dla Microelectronics Reliability, IET Circuits, Devices & Systems, Journal of the International Measurement Confederation, IEEE Transactions on Circuits and Systems-Part I (TCAS-I) Conferences: SIE10, ICSES 2010, ISCAS 2010, projects in the EU Operational Programme Innovative Economy 2.3
6. **Prof. A. Hławiczka**, grant proposals for the Czech Grant Agency (since 2000)
7. **Prof. E. Hrynkiewicz,** grant proposals for the Czech Grant Agency (since 2000); International Journal on Applied Mathematics and Computer Science; IFAC PDeS, IEEE – ICSES, IEEE DDECS Symposium, Conference on Reprogrammable Digital Devices
8. **Dr. J. Izydorczyk,** IEEE Transactions on Circuits and Systems I (TCAS-I), Studia Informatica, Pomiary Automatyka Kontrola, 8th International Conference on Education and Information Systems, Technologies and Applications EISTA 2010, IEEE International Symposium on Industrial Electronics ISIE 2010, International Symposium on Engineering Education and Educational Technologies EEET 2010, The Second International Conference on "Networked

Digital Technologies", eChalenges e-2010, International Conference on Signals and Electronic Systems ICSES 2010, 10th International IFAC Workshop on Programmable Devices and Embeded Systems PdeS

9. **Prof. D. Kania,** Computers and Electrical Engineering, Bulletin of the Polish Academy of Sciences – Technical Sciences, International Journal of Applied Mathematics and Computer Science, Microprocessors and Microsystems, Elektronika, Pomiary, Automatyka, Kontrola

10. **Prof. A. Karwowski,** IET Proceedings Microwaves, Antennas & Propagation (London); Electronic Letters; IEEE Transactions on Antennas and Propagation; IEEE Transactions on Microwave Theory and Techniques; International Symposium and Exhibition on Electromagnetic Compatibility (EMC)

11. **Dr. P. Kłosowski**, 2nd International Symposium on Engineering Education and Educational Technologies EEET 2010, grant proposoals in the Operational Program Innovative Economy 2007-2013 (Ministry of Science and Higher Education)

12. **Dr. D. Komorowski**, 32nd Annual International Conference of the IEEE Engineering in Medicine and Biology Society *"Merging Medical Humanism and Technology"*

13. **Dr. J. Konopacki,** IEEE International Conference on Signals and Electronic Systems

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19. **Dr. A. Pułka**, EU projects and project proposals (project Multicube supported be EU); Elsevier Journal: "Information and Software Technology"; IEEE International Conference on Signals and Electronic Systems 2010

20. **Prof. J. Rutkowski**, IEEE Transactions on Computer Aided Design (CAD)

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43. **Prof. E. Tkacz,** member of the International Advisory Board of the Annual Journal of Medical Informatics and Technology published by the University of Silesia
44. **Prof. E. Tkacz,** member of the Section Electronics at the Katowice Branch of the Polish Academy of Sciences

PATENTS AND PATENT APPLICATIONS

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1. **Piętka E., Kawa J.**, Advances in intelligent and soft computing 69, Springer, 2010, 625 pages

PUBLICATIONS OF THE INSTITUTE OF ELECTRONICS

1. **Filus Z., Hrynkiewicz E.**, Annual Review 2009 – Institute of Electronics, Gliwice, March 2010, 70 pages

ABSTRACTS OF SELECTED RESEARCH PROJECTS

DIVISION OF ELECTRONICS FUNDAMENTALS AND RADIO ENGINEERING

Z. Rymarski (DSc), *Single-phase and three-phase voltage source inverters for UPS systems*

The algorithm for a complete design of the single and three-phase VSI was the most important achievement of the research. The choice of the PWM type and its scheme (the sequence of the power switches control), based on a harmonic analysis of the unfiltered waveform of the voltage source inverter output and the graphical interpretation of this analysis for two separate frequency ranges in a function of the basic PWM parameters such as the modulation depth ratio and the carrier to fundamental frequency ratio has been justified. Simple formulas that enable the calculation of the output filter of the single or three-phase VSI have been worked out based on the limitations set on the output filtered voltage distortion level and on the minimisation of the reactive power in the output filter components. The ranges of parameters have been found for the single and three-phase VSI, namely the modulation depth ratio, parameters of the output filter and rectifier load with the R_OC_O filter, including parasitic parameters, for which it is possible to effectively decrease the output filtered voltage distortions for a nonlinear load. The output power stage, including the output filter, was described by means of difference equations for the different state variables vectors, taking into account the parasitic parameters of the filter and the previously calculated dependencies of the filter parameters on the carrier frequency and the nominal resistance load. The discrete PID/CDM controller was implemented in the inner inverter control loop, enabling sufficient robustness of the system for the load change by means of the choice of the proper time constant of the closed loop system. The RPC controller was implemented in the outer control loop, whose design was significantly simplified owing to the flat Bode characteristics of the inverter with the PID/CDM inner loop. The inner PID/CDM loop damps dynamic, aperiodic disturbances, the outer RPC loop is necessary for rejecting the periodic disturbances and minimizing the output voltage static error. The presented design algorithms were initially checked by means of simulations and finally verified by means of the experimental model. The VSI design described was compared with the voltage source inverters controlled by means of alternative methods well known from references and the results of simulations were similar.

T. Topa (Ph.D), Prof. A. Karwowski, A. Noga (Ph.D.), *Using GPU with CUDA to Accelerate MoM-Based Electromagnetic Simulation of Wire-Grid Models*

Wire-grid modelling of conducting bodies has been one of the most noteworthy paradigms of computational electromagnetics. The concept dates from the mid-sixties, and consists in approximating the continuous body surface by a wire mesh. The wire-grid approach combined with integral equation formulations and the method of moments (MoM) proved its great capabilities in a wide variety of far-field scattering and radiation problems involving arbitrarily shaped conducting bodies and wires. Unfortunately, MoM-based numerical simulation computer codes suffer from their high demands of computer resources needed to perform computations. Therefore, traditional single-CPU sequential MoM codes can potentially greatly benefit from employing GPGPU computing model (General-Purpose computing on Graphics Processing Unit), i.e., using a GPU for computational tasks not just related to graphics processing but for those traditionally performed by the CPU. Wire-grid MoM codes seem to be especially worth the effort of porting them, at least partially, to GPU, since they combine flexibility, robustness, usefulness and effectiveness with relative ease of implementation of relevant algorithms.

Within this research, we demonstrated the possibility of accelerating the MoM-based electromagnetic simulation of wire-grid models of radiating/scattering structures using GPU CUDA hardware. For the GeForce GTX 275 from NVIDIA used in this study, the improvement in performance with a speedup ratio of about 6x is achieved (for a medium-size problem with 5783 unknowns) compared to the reference CPU single-core implementation of the MoM code. It should be emphasized that the measured GPU runtimes have included the overhead time on data transfer forth and back between the host and GPU device as well as the time penalty for data pre- and post-processing on CPU, initializing kernels, etc. Thus, the speedup ratio of 6x represents a real indication of the speedup practically attainable for the considered class of problems and relevant computer codes.

J. Fiołka (PhD), Z. Kidoń (PhD), *Analysis of stabilographic trajectories using time-frequency techniques*

Stabilography is a non-invasive diagnostic method used to analyze human postural stability. Human posture can be quantified by measuring – with the aid of a static force platform – the movement of the center of pressure (COP) under the patient's feet. The COP coordinates are derived from the knowledge of the locations of the transducers and registered ground reaction forces. The trajectory, that describes the movement of the COP in the anteroposterior/mediolateral plane, is registered during the 30 up to 120 seconds trial time. The direct examination of the trajectory has limited application due to the time consuming nature of this visual analysis. For this reason, many different parameterization methods have been used in a clinical assessment. In a classical approach, postural stability is estimated by computing parameters such as the length

and area of a trajectory, maximal sway in anteroposterior and mediolateral direction, mean velocity of the COP etc. The main disadvantage of this approach is that it does not provide an information about the dynamics and structures of the process.

The work presents an attempt to characterize postural stability with the use of time-frequency analysis. Time-frequency (TF) signal representations characterize signals on the time-frequency plane. The most popular TF distributions are: spectrogram (squared magnitudes of the short-time Fourier transform), scalogram (squared magnitudes of wavelet transform) and a group of bilinear distributions (e.g. Wigner, Cone-shape, Choi-Williams distribution). As was shown, the selection of the time-frequency representation is rather crucial. To identify the dynamic changes of the COP signal, TF distribution should have a high resolution in the joint time and frequency domain and should reduce cross-terms interferences. On the basis of the performed tests it can be concluded that the Choi-Williams distribution is suitable for the stabilographic signal analysis.

The research project has been also focused on the application of the wavelet transform to the human postural stability analysis. The wavelet transform, that belongs to a class of linear time-frequency representation, has been proved to be a successful tool for analysis of biomedical signals because of its good localization properties and ability to detect self-similarity in analyzed signals. In the study, the procedure for construction of scaling functions and wavelets - well adapted to the structures of the stabilographic signals - was developed. Thanks to that we are able to increase the efficiency of the proposed method by using wavelets that are better "fitted" to the analyzed signal than commonly used wavelets, such as Daubechies, Coiflets, Symlets family. In the work, a special attention was paid to the development of methods for parameterization of the stabilographic trajectory. The human posture control systems are characterized by the Hurst exponent and the log-log plot (variance of the detail coefficients vs. decomposition level). Moreover, a new parameter FV (Fitting Violation) was introduced to describe how well the regression line fits the data. Among the different measures of goodness-of-fit the root mean squared error (RMSE) was used. To confirm the usefulness of the used definitions, a detailed study was performed to explore the discriminative potential and reliability of the proposed parameters.

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

R. Czerwiński (PhD), Prof. D. Kania, *A synthesis method of high speed finite state machines*

This work concerns the problem of state assignment and logic optimization of high speed finite state machines. The method is designed for PAL-based CPLDs implementations. Determining the number of logic levels of the transition function before the state encoding process, and keeping the constraints during the process is the main problem at hand. A number of coding bits, as well as codes for the states, are

adjusted to achieve a machine with a determined number of logic levels. The research work concerns two problems: PAL-oriented state assignment and PAL-oriented two-level optimization of output block.

Considering the FSM realization, dedicated for PAL-based CPLDs, the number of implicants of every single function should fit the number of product terms best. So, the number of implicants should be known in the process of state assignment. Of course the number of terms may be reduced as the effect of two-level minimization. The main goal of the state assignment process should be to assign states with codes conveniently situated for minimizer. It is complicated for FSMs, because the input parts of the multi-output implicants are connected with the output part. The next state of the transition is the present state of another transition. Changing one bit of the state code involves changes in both input and output part of the implicants. On the other hand, elements of two-level minimization must be included in the state assignment process, in order to take advantage of the number of the PAL-based cell terms. The developed primary and secondary merging conditions enable to include elements of two-level minimization into the process of the state assignment.

The concept of two-level optimization of FSM's output block lies in the background of the original method of product term expansion utilizing tri-state buffers. Classical logic synthesis of combinational circuits implemented in a great majority of vendor tools consists of two steps. First a two-level minimization is applied separately to every single-output function. Then, implementation of the minimized functions in PAL-based blocks, containing a predefined number of product terms, is performed. If the number of implicants, representing a function after minimization, is greater than the number of product terms, product term expansion is executed. The classical product term expansion method consists in utilizing feedback lines to build a multi-level cascaded structure, which increases propagation delays significantly. Product term expansion that exploits tri-state output buffers seems to be the most attractive solution, because it does not lead to expansion of logic levels.

M. Chmiel (PhD), R. Czerwinski (PhD), Prof. E. Hrynkiewicz, J. Kulisz (PhD), J. Mocha (MSc), *A bit-word PLC development platform*

The work was concentrated on the hardware-software platform designed in order to test different constructions of the central processing units dedicated to programmable logic controllers. Selected hardware solutions for the PLC dual processor bit-byte (word) CPUs, which are oriented for optimized maximum utilization of capabilities of the two-processor architecture of the CPU are investigated. The key point is preserving high speed of instruction processing by the bit-processor and high speed and functionality of the byte (word)-processor. The structure should enable the processors to work in the concurrent mode as far as it is possible, and minimize the situations when one processor has to wait for the other. The designed platform is based on the development board equipped with Xilinx Virtex-4 FPGA. A software tool for testing possibilities of the selected units and testing utilization of the programmable structure was also developed.

Moreover the hardware and software tools used to support Programmable Logic Controller (PLC) program testing and verification were considered. As a result the idea of a PC-based object simulator was elaborated. The simulator consists of a PC equipped with an appropriate I/O card, and a simulator program running on the PC. The simulator is capable of emulating behavior of real industrial objects. Thus a significant part of software tests can be executed with using the simulator, instead of a physical object. This can significantly facilitate and accelerate the development of an application.

Prof. A. Hławiczka, T. Garbolino (PhD), K. Gucwa (PhD), *Size Reduction of Signature-based Diagnostic Dictionary Used for Testing of Connections*

The work deals with a novel and advanced method intended to reduce the size of a diagnostic dictionary that is used for detection, localization and identification of static and delay faults in interconnections that are tested by means of specific Interconnect BIST (IBIST) structure. The IBIST has a form of a ring register R-LFSR of which the feedback lines constitute the connections under test. The previous studies of the authors assumed implementation of a single 2n-bit R-LFSR structure for testing and diagnosis of faults occurring in buses with the width $n \leq 32$ bits. As the size of the diagnostic dictionary rapidly grows in pace with both the number of connections under test and increase of the fault-multiplicity, it was a significant drawback that hindered examination of very wide buses.

The problem has been solved by splitting the n-bit bus into b fragments with the width of k bits each. Every fragment is tested by an independent R-LFSR register with its length of 2k bits. The study assumes faults with the maximum fault-multiplicity rmax=3 for each k-bit fragment of the bus, where the faults present combinations of stuck-at 0/1, AND /OR shorts of two or three lines and delay faults. In addition, the test procedure is subdivided into four phases whereas odd and even R-LFSRs are activated alternately. It is the way of subdivision that makes it possible to get rid of the mutual interference between two adjacent R-LFSRs when a short between feedback lines of these neighboring registers takes place. Likelihood of such interactions presented the impediment that prevented the fault dictionary from having its size reduced.

The innovative solution that is suggested in this study enables to substantially diminish the dictionary, where its actual size is determined by the multiplicity of r defects within each k-bit part of the connecting bus, even when the bus width $n >> k$. It was achieved by substantial reduction of the number of signature entries covered by the dictionary as well as by shortening the length of the signatures b times. Moreover, the newly developed method enables to locate and identify substantial part of faults for the entire bus with the width of n, where the multiplicity of faults can be even as high as $b\ r_{max}$.

DIVISION OF CIRCUIT AND SIGNAL THEORY

Prof. J. Rutkowski, K. Mościńska (PhD), P. Jantos (PhD), *Increasing teaching efficiency in engineering courses based on Bloom's taxonomy*

There have been many attempts to categorize learning outcomes. These are broadly referred to as taxonomies of learning and can be useful ways of stating what students are expected to achieve. Bloom identified six levels within the cognitive domain, from the simple recall or recognition of facts, as the lowest level, through increasingly more complex and abstract mental levels, to the highest order which is classified as evaluation. For students to progress up the hierarchy, they must function at lower levels firstly, incorporating that level of activity, and then proceed up through each level to more complex functioning. Students of technical courses should be able to achieve all lower level abilities (knowledge, understanding), as well as – depending on the year of study – most of higher level competences, for instance evaluation and synthesis (generate, assemble, design, compare, correct).

Circuit Theory is an obligatory, two semester course delivered to all students of the Faculty of Automatic Control, Electronics and Computer Science, Gliwice, Poland. Since 2005, the course is delivered in the blended e-learning version. In the last few years we have observed increasing problems with the laboratory work - students neither possess theoretical background of an exercise, nor can perform successfully measurements and interpret the obtained results. The goal of our study was to identify main reasons of students' poor performance in the laboratory. We have verified whether all course components enable sufficient preparation for the laboratory work. We have also analysed the contents of laboratory exercises and pre-lab short tests in order to find out which levels of knowledge they address. Bloom's taxonomy of learning outcomes has been applied in order to classify questions and problems into categories. In general, disregarding of the Bloom's pyramid structure was found out as the leading source of laboratory failure - lack of lower level knowledge components inhibits application of medium level elements and therefore prevents successful execution of laboratory exercises. The authors have suggested modification of the laboratory program so that all practical work was preceded by obligatory calculations (calculate – assemble exercises). Moreover, we have introduced weekly obligatory computer quizzes, to be solved before attending laboratory exercises. We have focused on graded difficulty of problems, in order to represent particular levels of Bloom's taxonomy. Such a form of formative assessment lets students gain more experience and build self-confidence. Most students confirm that the introduction of quizzes enables better preparation for the laboratory as well as gradation of difficulty level helps to understand the course. Adequate difficulty level of pre-lab tests (including lower level cognitive categories – knowledge, comprehension) and focusing on practical issues is necessary in order to decrease students' failure rate and improve students' attitude to technical courses.

T. Golonek (PhD), D. Grzechca (PhD), *Analog fault diagnosis by means of supply current monitoring*

The designed technique allows to identify diagnostic states of an analog circuit under test (CUT) by means of quiescent supply current monitoring (I_{DDQ} testing). The supply current I_{DD} of an integrated CMOS circuit is minimal for a healthy structure (equal to the sum of MOS transistors leakage currents) and grows radically for a hard fault presence (e.g. SiO_2 layer punctuation). The obvious advantage of I_{DDQ} testing is that it does not require access to inner nodes of the structure. In contrary to the versions of I_{DDQ} testing techniques published previously, the proposed one determines the set of optimal test points (e.g. supply voltages, levels of excitations) in an evolutionary system. Thanks to this process, the supply current of the CUT is monitored only in these test points which are necessary to achieve the possible highest faulty states separation, so the testing time has been reduced radically. For example, the number of the observed points of I_{DD} for the tested operational transconductance amplifier (OTA) has been reduced from 286 points to 8 points. Besides, the method uses the ambiguity sets (AS) concept, which assures resistance of the approach to practical inaccuracies (e.g. measurements and excitations impreciseness). The applied genetic algorithm (GA) system uses the binary matrix representation of genotypes for solution coding. Additionally, to improve the convergence for the optimal phenotype, the coding map is optimized during evolutionary computations that allows to achieve the resistance of the desired schemes to destruction during recombination process.

A. Pułka (PhD), A. Milik (PhD), J. Konopacki (DSc), *Hardware implementation of selected digital filters in the programmable logical structures*

The main objective of the research work was to find an optimal implementation of digital filters in FPGA structures. The authors proposed a new methodology of digital IIR and FIR filters implementation. The FIR and IIR structures were optimized for the best utilization of circuits resources. The modern modelling and cosimulation environment Aldec's Active-HDL with MATLAB were used to complete the entire task. FIR filters were designed by means of MATLAB's Parks McClellan procedures, whereas for IIR filters the design methodology based on the optimal approximation of the prescribed magnitude and phase responses was used. This method was implemented in MATLAB together with the original formulas for a filter order and a group delay estimation. This approach guarantees IIR filters stability and small magnitude overshoot (usually less than 1 dB). The obtained filter structures were analyzed towards their computation complexity and the final results of this analysis were validated by the logic synthesis of IIR and FIR in FPGA devices.

DIVISION OF TELECOMMUNICATION

J. Izydorczyk (PhD), *Modelling the nonuniform transmission line for SPICE transient analyses*

This work has been devoted to the elaboration of an analysis method of the nonuniform transmission line (NUTL) with the utilization of a typical circuit simulator like SPICE. It is assumed that quasi-TEM modes are propagated in the nonuniform transmission line. The solution of the problem is divided into three parts. 1) The analysis of a nonuniform transmission line is reduced to the analysis of cascaded sections of the linear varied nonuniform transmission line (LNTL). The proper algorithm originates from literature. 2) A omputational model of the linear varied nonuniform transmission line is elaborated following the asymptotic waveform evaluation methodology. The q-pole model is matched to imitate position of zeros and poles of admittance matrix of the nonuniform transmission line. 3) A synthesis of a passive circuit which implements the model for a broad range values of the linear varied nonuniform transmission line slope constant. Consequently the parameters of the circuit can be evaluated precisely as a polynomial function of the slope constant. The method reduces the nonuniform transmission line to cascaded linear varied transmission lines. Linear varied nonuniform transmission line segments are approximated by a passive circuit, which consists of an inductance cascaded with the Darlington C section. The model is implemented in the circuit simulator as a passive circuit. Parameters of each section are computed using polynomial regression. Cascaded circuits are insensitive to parameters variation. Due to this fact inevitable regression errors do not disturb frequency response of the model significantly.

G. Dziwoki (PhD), *The analysis of the Reduced Constellation Decision-Directed blind phase correction method*

Phase offset recovery, besides channel equalization and timing synchronization, belongs to important tasks performed in the physical layer of communication receivers. Correct information symbol detection is impossible without accurate phase estimation even if no intersymbol interference exists. The simplest blind phase offset recovery scheme is based on the decision-directed method and an idea of reduced constellation. The reduced constellation consists of four reference symbols, one for each quadrant of the complex plane. The common working principle of the blind phase recovery scheme relies on minimization of the distance between a received distorted symbol and the nearest symbol taken from the reduced constellation, providing that the amplitude value of the received symbol is above a predefined activation threshold.

The aim of the research is examination of some features of the RCDD method in the case of 64-QAM signal constellation. The cost function of the phase recovery scheme with a reduced constellation approach is considered as well as a way of its application in an adaptive algorithm. A comparison between different versions of decision-directed approach is made . The performed experiments show the influence of the activation

threshold on the phase correction efficiency. On the basis of performed simulations and mathematical transformations some interesting remarks on the analyzed methods have emerged:

In the idea of the reduced constellation all received signals can be used in the phase update. There is no need to use the activation threshold value for correct work of the RCDD algorithm, the MSE (Mean Square Error) cost function has a sinusoidal-like shape, especially in presence of noise and channel distortion. The minimum point corresponds to good estimation of the correct phase value.

The implementation of the RCDD method only requires sign detection of the received signal and the computation of difference between the absolute values of real and imaginary parts of this signal.

W. Sułek (PhD), *Optimization of LDPC decoder implementation*

The outstanding error correction performance and highly parallel iterative decoding algorithms have made Low-Density Parity-Check (LDPC) codes the most powerful error correcting codes for reliable high speed communication applications. They have been recently adopted for a variety of industrial standards. Besides all their desirable properties, one characteristic of LDPC codes, namely the randomness of parity-check matrix structure, makes implementation of LDPC decoders a difficult task as it leads to complex interconnect wiring for practical codes, and hence to large demands for hardware resources in a decoder implementation. Thus the implementation of high performance decoders is still a demanding task.

The research project concerns the hardware iterative decoder for a subclass of LDPC codes that are implementation oriented. They are known as Architecture Aware LDPC (AA-LDPC). The decoder has been implemented in a form of parameterizable VHDL description. Current research is focused on optimization of decoder implementation, i.e. throughput increasing as well as hardware resources savings. To achieve a high clock frequency of the decoder hardware implementation, a large number of pipeline registers has been used in the processing chain. However, the registers increase the processing path delay, since the number of clock cycles required for data propagating is increased. Thus in general a number of idle cycles must be introduced between decoding sub-iterations. We have provided a method for calculation the exact number of required idle cycles on the basis of parity check matrix of the code. The main contribution of this work is a heuristic algorithm for parity check matrix optimization to minimize the total number of required idle cycles and hence maximize the decoder throughput. The proposed matrix optimization method does not change the code properties, however the decoder throughput can be significantly increased.

Significant part of the decoder area is occupied by Configurable Interconnection Network. The network consists of a set of multiplexers that propagate the data from the memory to the computation units. Behavioral description of the interconnection network gives quite poor synthesis results: the decoder area is large and exponentially

dependent on the number of inputs/outputs. Instead of straightforward behavioral description, the switching network can be described structurally, making use of ideas known from the theory of telecommunication interconnection networks: Benes or Banyan switches. We developed the interconnection network implementation based on the Banyan switch with an additional multiplexer stage to enable non-power-of-2 numbers of outputs. Comparison of synthesis results for the network with behavioral description as well as the Banyan structural description shows a significant advantage of the proposed Banyan network.

DIVISION OF BIOMEDICAL ELECTRONICS

M. Kotas (PhD), *Spatio-temporal filtering for fetal electrocardiogram enhancement*

The electrocardiographic technique of fetal heart rate monitoring, based on maternal abdominal electrodes, has attracted researchers' attention for many years. The first important reason of such an activity is that the technique is really noninvasive. The second, that it determines precisely the time locations of the fetal heart contractions and thus provides more accurate information on the instantaneous fetal heart rate than the widely used instrumentation based on the Doppler ultrasound technique. However, the low energy level of the fetal electrocardiogram (FECG) recorded from the maternal abdominal wall and the presence of the noise components of much higher energy can often prevent successful analysis of the signal. This is why the clinical diagnostic applications of this technique are rather limited. Still, the research should be continued to overcome the problems related to the FHR determination on the basis of the maternal abdominal bioelectric signals.

These signals contain the maternal electrocardiogram (MECG), the fetal electrocardiogram and different types of noise. Since the MECG amplitude significantly exceeds that of the desired FECG, the primary operation is the maternal ECG suppression. Two most important approaches to cope with this problem can be distinguished. The first one exploits the repeatability of ECG beats to achieve the goal. The second approach is based on spatial filtering of the multi-channel abdominal signals: the singular value decomposition (SVD) and the independent component analysis (ICA) are successful in maternal and fetal ECG signals separation. However, our previous experiments showed that when a small number of channels was recorded, it was more advantageous to apply the single-channel approach (based on template subtraction).

In this work we propose a new structure of the instrumentation for electrocardiographic fetal monitoring. We apply a single-channel approach to maternal electrocardiogram suppression in the recorded four abdominal bioelectric signals. Suppression of the MECG in the individual channels allows us to apply the weighted summation of the respective channels, i.e. their spatial filtering, to FECG component enhancement. Moreover, summation of the consecutive signal samples of the respective channels can

be used to exploit not only spatial distribution of the signal, but also its temporal properties. This approach, the spatio-temporal filtering of the FECG signal, is the main proposition of this work. It is applied to construct a new channel with higher signal-to-noise ratio. Finally, we perform detection of fetal QRS complexes. The proposed approach was investigated with the help of the constructed database of the maternal abdominal signals. In the detection tests, the spatio-temporal filtering allowed us to decrease the number of the detection errors by more than twice. Moreover, we presented visually that even if the fetal QRS complexes are buried in noise, the spatio-temporal filtering can produce the signal with the discernible ones.

Prof. J. Łęski, N. Henzel (PhD), *Generalized Ordered Linear Regression with Regularization*

From the times of A. Legendre and K. Gauss the least sum of squares (least squares in short) method is an essential tool in the experimental sciences such as astronomy, biology, physics, sociology, psychology, naming just a few of them. The method had also a major impact on the development of the estimation theory. Currently, the method is routinely applied in signal processing, pattern recognition, machine learning, system identification, fuzzy systems, neural networks and elsewhere, where we analyze distorted data. Despite the fact that more than 200 years have passed, the least squares criterion is still the most widely used one due to its elegant analytical solution that requires low computational effort. However, it is well known that this method is optimal only for normal (Gaussian) density function of model residuals. In general, for nongaussian noise the maximum likelihood estimator is optimal when the squared residuals are replaced by another function of the residuals, that is, the negative logarithm of the probability density function of the residuals.

Linear regression analysis has become a fundamental tool in experimental sciences. We propose a new method for parameter estimation in linear models. The 'Generalized Ordered Linear Regression with Regularization' (GOLRR) uses various loss functions (including the epsilon-insensitive ones), ordered weighted averaging of the residuals, and regularization. The algorithm consists in solving a sequence of weighted quadratic minimization problems where the weights used for the next iteration depend not only on the values but also on the order of the model residuals obtained for the current iteration. Such a regression problem may be transformed into the iterative reweighted least squares scenario. The conjugate gradient algorithm is used to minimize the proposed criterion function. Finally, numerical examples are given to demonstrate the validity of the method proposed.

E. Straszecka, (PhD), *Medical diagnosis support by means of uncertainty and imprecision measures*

It is proposed to base diagnosis support on three theories: the fuzzy set theory and the related possibility theory, as well as the Dempster-Shafer theory. The theories are

combined in such a way that both imprecision of premises and uncertainty of diagnostic hypotheses are considered. The inference is done for heuristic rules `If symptom(s) then diagnosis'. Premises of these rules are represented by fuzzy sets and their weights by values of the basic probability assignment defined in the Dempster-Shafer theory. A matching level between the premise and a patient's finding is determined during a consultation. The matching level is defined by means of the possibility theory. Rules for which the matching level between the premise and an observation is greater than the assumed threshold are activated during the inference and their conclusions are considered diagnostic hypotheses. The hypothesis with the greatest belief value is the final conclusion. This method of diagnostic inference seems to be close to intuitive understanding of diagnosis support by physicians. However, it requires developing the Dempster-Shafer theory to enable the representation of focal elements by fuzzy sets as well as a modification of information combining. The existing methods of combining information bring inconsistent results. The proposed method allows for joining information from different sources, with simultaneous elimination of incoherent symptoms. Thus, the same knowledge base can be used in different circumstances, for instance when diagnostic procedures were changed, which is a prerequisite for knowledge transfer. The proposed methods are verified for the Internet and individually gathered data.

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

Z. Pruszowski (PhD), P. Kowalik (PhD), *Preparation of stable resistive layer of metal plating method*

Amorphous alloys containing nickel, cobalt, copper or transition metals such as tungsten or molybdenum, and additives such as solid-state phosphorus or boron, are materials widely used in electronics for the production of film resistors. Resistors produced in this way are characterized by:

- Temperature coefficient of resistance (measured both in the range 218 ÷ 293K and in the range 293 ÷ 398K) is low, not greater than 25ppm/K
- Long term stability (measured after 1000 hours at 343K when the rated current flowed through the resistor, and after 1000 hours at 428K without the flow of the rated current) is less than 0.5% of the relative change in resistance.

The result of the process carried out at a constant temperature (368K) and a constant acidity of the solution of pH = 2.0, is the alloy Ni-P whose composition is Ni = 80.5 ÷ 80.8% atomic, P = 19.2 ÷ 19.5% atomic, and which crystallizes to Ni3P-Ni eutectics. As stated, this composition can minimize TCR of Ni-P and raises the temperature of phase transition amorfit-crystallite which and such a composition is suitable for applications in the electronics industry.

The results obtained in the work can be characterized by the following:

- resistive amorphous alloys Ni-P obtained by electroless metallization technology feature good stability of resistance
- resistance dependence on temperature is described by the second-degree polynomial which gives a linear dependence of TCR on temperature. This means that the temperature rise moves the value of TCR towards positive values.

M. Kwoka (PhD), N. Waczyńska (MSc), M. Sitarz(MSc), Prof. J. Szuber, *XPS and TDS comparative studies of L-CVD SnO_2 ultra thin films*

In this project we performed comparative studies of the chemical stability of L-CVD SnO_2 ultra thin films (20 nm) deposited on the atomically clean Si(100) substrate after their subsequent in situ hydrogenation and oxidation, and then after exposure to air. For the control of surface chemistry of these films we used in a comparative way the X-ray Photoemision Spectroscopy (XPS) combined with ion depth profiling (DP XPS) and Thermal Desorption Spectroscopy (TDS).

Our XPS experiments showed that the L-CVD SnO_2 ultra thin films after subsequent in situ hydrogenation and oxidation consist of a strongly nonstoichiometric layer at the top of Si dioxide substrate. After subsequent exposure to air they were covered with undesired 3 monolayers of C contamination and various forms of oxygen. During the TDS procedure a two-step desorption of molecular hydrogen (H_2), water vapour (H_2O), carbon dioxide (CO_2) and atomic oxygen (O) at the temperature of ~ 530 K and 600 K was observed, respectively. It was in a good correlation with evident decreasing of the relative concentration of C contaminations, as well as variation of nonstoichiometry of the L-CVD SnO_2 ultra thin films as determined by XPS combined with ion depth profiling.