Silesian University of Technology
Faculty of Automatic Control, Electronics and Computer Science

Annual Review 2006

Institute of Electronics

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Edited by
Maria Drelichowska

Institute of Electronics, March 2007

FOREWORD

The Institute of Electronics is a part of the Faculty of Automatic Control, Electronics and Computer Science, one of the 12 faculties of the Silesian University of Technology, founded in 1945. The University is located in Gliwice and has about 31,000 students at present. The Faculty of Automatic Control was founded in 1964, and after a few reorganisations it changed its name to the Faculty of Automatic Control, Electronics and Computer Science. Since its creation in 1974 the Institute of Electronics has been involved in various research and teaching activities. The Institute has about 100 members of academic staff and consists of six divisions:

- ***Division of Electronics Fundamentals***
- ***Division of Digital and Microprocessor Systems***
- ***Division of Circuit and Signal Theory***
- ***Division of Telecommunication***
- ***Division of Biomedical Electronics***
- ***Division of Microelectronics and Biotechnology***

The Institute specialises in such advanced fields of engineering as analogue and digital electronic systems, including biomedical systems, production of telecommunication and electronic systems etc. Research in these areas ranges from component to system level, encompassing practical and theoretical investigations with the application of both hardware and software techniques. Research groups are supported by a wide range of test and instrumentation equipment together with computer facilities, which can run with programming languages of all levels and offer various application software. Many of the Institute's research programmes are carried out in close co-operation with industry in order to satisfy the needs of the region, which is the main industrial centre of Poland.

The Institute offers two-stage five-year courses leading to the degree of MSc, which is obtained on the basis of a project and a report, presented during a final examination. After the first stage of study, lasting three and a half years, students can complete their education and leave the university with the BSc degree. The Institute participates also in a five-year MSc course in Automatic Control, Electronics and Computer Science, run by the Faculty, in which all teaching is in the English language. The courses normally consist of lectures, laboratories, seminars and projects, and are followed by examinations. Apart from this, the Institute offers five-year courses at evening studies, leading to the degree of BSc. The curricula of the courses run by the Institute are designed for people who want to achieve both theoretical knowledge and practical skills in electronics. At present, the total amount of students is about 1100. Other didactic activities include postgraduate and PhD studies.

The following pages provide detailed information regarding the research carried out as well as the subjects taught in each division.

CONTENTS

DIRECTORS OF THE INSTITUTE

Director of the Institute:

Prof. Edward HRYNKIEWICZ

Vice Director of the Institute for Research:

Prof. Zdzisław FILUS

Vice Director of the Institute for Teaching:

Dr. Lucjan KARWAN (until 31 August 2006)
Dr. Adam BŁASZKOWSKI (from 1 September 2006)

DIVISION OF ELECTRONICS FUNDAMENTALS

Head of Division: Prof. Zdzisław Filus, PhD, DSc

Research staff

Prof. Zdzisław FILUS, PhD, DSc

Prof. Andrzej KARWOWSKI, PhD, DSc
Prof. Leon LASEK, PhD, DSc

Adam BŁASZKOWSKI, PhD
Andrzej BŁONAROWICZ, PhD
Jacek CHĘCIŃSKI, PhD
Władysław CIĄŻYŃSKI, PhD
Jerzy FIOŁKA, PhD
Zenon KIDOŃ, PhD
Adam KRISTOF, PhD
Sławomir LASOTA, PhD
Mirosław MAGNUSKI, PhD
Andrzej MALCHER, PhD
Wojciech OLIWA, PhD
Zbigniew RYMARSKI, PhD
Maciej SURMA, PhD
Włodzimierz SZMELCER, PhD
Grzegorz WIECZOREK, PhD
Dariusz WÓJCIK, PhD

Piotr ZASTAWNIK, MSc

PhD Students

Artur NOGA, MSc
Tomasz TOPA, MSc

Research fields

- Electronic circuits synthesis
- Symbolic methods of electronic circuits analysis
- Electronic circuits for automotive applications
- Measurement of selected physical quantities based on eddy current methods
- Intrinsically safe power supply modules with increased power rating
- Microprocessor-based measurement systems
- Computational electromagnetics
- Numerical modelling of radiating and scattering wire objects
- Linear antenna theory
- Electromagnetic compatibility
- Optoelectronics, Fiberoptics

Courses

- Semiconductor Devices
- Analogue Electronic Circuits
- Analogue Circuits Design
- Electronic Measurement Techniques
- Switching Circuits
- Special Semiconductor Devices and Circuits
- Materials Technology and Electronic Equipment Design
- Field and Wave Electromagnetics
- Introduction to Radio Communication
- Radio Engineering Systems
- Fields, Waves and Antennas
- Wireless Computer Networks
- Design of Radio Electronic Devices
- High-Frequency Engineering Fundamentals
- Electromagnetic Compatibility

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

Head of Division: Prof. Edward HRYNKIEWICZ, PhD, DSc

Research staff

Prof. Edward HRYNKIEWICZ, PhD, DSc

Prof. Andrzej HŁAWICZKA, PhD, DSc
Assistant Prof. Zdzisław POGODA, PhD

Mirosław CHMIEL, PhD
Robert CZERWIŃSKI, PhD
Tomasz GARBOLINO, PhD
Krzysztof GUCWA, PhD
Eugeniusz KOSEK, PhD
Józef KULISZ, PhD
Adam MILIK, PhD
Maciej NOWIŃSKI, PhD
Adam PAWLAK, PhD
Krzysztof PUCHER, PhD
Tomasz RUDNICKI, PhD
Wojciech SAKOWSKI, PhD
Dariusz STACHAŃCZYK, PhD
Krzysztof TABOREK, PhD
Bernard WYRWOŁ, PhD

Dariusz POLOK, MSc

Research fields

- Testing and testability of digital systems
  - Generation of test patterns
  - I_{DDQ} testing
  - Design for testability
  - Built-in self-tests and concurrent testing
  - Pseudorandom techniques for built-in tests for VLSI circuits and design of standard P1149 compatible chips
  - Microcomputer signature analysis
- Design of systems with PLDs, FPGAs and programmable controllers
  - Design of support software
  - Logic synthesis
  - Implementation of logic structures in CPLDs, FPGAs and PSoCs
  - Fast operating CPU structures of programmable controllers and methods of PLC programming

  - Distributed structures of PLCs
  - PLC applications
- Frequency multipliers based on digital techniques
- Laboratory and industrial data acquisition and control systems
  - Signal conditioning
  - Analogue-to-digital and digital-to-analogue converters with optical isolation and fibre optic transmission systems
- Multiprocessor systems
  - Pipelining and parallel processing
  - Systems with global memory and arbitration
  - Statistical analysis of performance for pipelining processing
- ASIC design
  - High level design methodologies
  - System modelling and simulation (using VHDL and Verilog)
  - Distributed design methodologies based on Internet

Courses

- Digital Systems Fundamentals
- Design of Digital Devices
- Microprocessors Fundamentals
- Microprocessor Systems
- Reliability and Testing of Electronic Devices
- Computer Aided Design of Integrated Circuits
- Programmable Logic Devices
- Programmable Controllers

DIVISION OF CIRCUIT AND SIGNAL THEORY

Head of Division: Prof. Jerzy RUTKOWSKI, PhD, DSc

Research staff

Prof. Jerzy RUTKOWSKI, PhD, DSc

Tomasz GOLONEK, PhD
Tadeusz GRABOWIECKI, PhD
Damian GRZECHCA, PhD
Lucjan KARWAN, PhD
Jacek KONOPACKI, PhD
Jan MACHNIEWSKI, PhD
Katarzyna MOŚCIŃSKA, PhD
Andrzej PUŁKA, PhD

PhD Students
Łukasz CHRUSZCZYK, MSc
Paweł JANTOS, MSc

Research fields

- Computer-aided electronic circuits analysis and design
  - Failure diagnostics in analogue electronic circuits
  - Application of sensitivity methods to the analysis and synthesis of electronic circuits
  - Modeling and simulation of digital and mixed analog-digital circuits in VHDL language
  - System level design in SystemC
  - Application of artificial intelligence methods and genetic algorithms to circuit theory and electronics
  - Common-sense reasoning modeling and application of AI techniques to circuits models generation and verification
- Signal processing and basic research into neural networks (analysis, synthesis and optimization) and their application to engineering practice
  - Application of neural networks to image processing and recognition, including texture images
  - Application of wavelet techniques to signal processing
- Web – based education

Courses

- Circuit Theory
- Signal Theory
- Fundamentals of Electrical Engineering
- Information Theory and Coding
- Computer-Aided Design of Electronic Circuits
- Digital Signal Processing
- Neural Networks

DIVISION OF TELECOMMUNICATION

Head of Division: Dr. Jacek IZYDORCZYK

Research staff

Jacek IZYDORCZYK, PhD
Dariusz KANIA, PhD, DSc

Adam DUSTOR, PhD
Maria DZICZKOWSKA, PhD
Leszek DZICZKOWSKI, PhD
Grzegorz DZIWOKI, PhD
Piotr KŁOSOWSKI, PhD
Marcin KUCHARCZYK, PhD
Andrzej KUKIEŁKA, PhD
Jerzy WOJTUSZEK, PhD
Piotr ZAWADZKI, PhD

PhD Students
Paweł BADURA, MSc
Mariusz BĄK, MSc
Wojciech SUŁEK, MSc

Research fields

- Digital commutation in modern telecommunication systems
  - Construction of telephone exchanges
  - Supervisory software for telephone exchanges
  - Special services (e.g. teleconferences)
  - Implementation of digital networks with integrated services (ISDN, B-ISDN, ATM)
- Application of digital signal processing to telecommunication
  - Compression of speech signal with the application of DSPs
  - Speech synthesis
  - Speech and speaker recognition
  - Application of artificial neural networks to signal processing
  - Design, testing and implementation of error correcting and modulating codes
  - Design of modern local area networks
  - Implementation and testing of new services in the Internet
  - xDSL technology

- Electromagnetic field engineering
  - Radiation and scattering of electromagnetic waves
  - Lightning protection
- Modems

Courses

- Fundamentals of Analogue and Digital Communication
- Fundamentals of Commutation
- Switching Nodes and Exchanges
- Principles of Transmission
- Communication Systems
- Signal Theory
- Information Theory and Coding
- Digital Signal Processing
- Computer-Aided Analysis of Electronic Circuits
- Digital Signal Processors (DSP)
- Neural Networks
- Computer Networks
- Internet
- Modems
- Introduction to Cryptography

DIVISION OF BIOMEDICAL ELECTRONICS

Head of Division: Prof. Jacek ŁĘSKI, PhD, DSc

Research staff

Prof. Jacek ŁĘSKI, PhD, DSc
Prof. Ewa PIĘTKA, PhD, DSc

Robert CZABAŃSKI, PhD
Arkadiusz GERTYCH, PhD
Norbert HENZEL, PhD
Jerzy IHNATOWICZ, PhD
Marian KOTAS, PhD
Tomasz PANDER, PhD
Stanisław PIETRASZEK, PhD
Sylwia POŚPIECH-KURKOWSKA, PhD
Tomasz PRZYBYŁA, PhD
Ewa STRASZECKA, PhD
Wojciech WIĘCŁAWEK, PhD
Piotr ZARYCHTA, PhD

PhD Students
Michał JEŻEWSKI, MSc
Jacek KAWA, MSc
Dominik SPINCZYK, MSc

Research fields

- Biocybernetics and biomedical engineering - processing of information in medicine
  - Processing of biomedical signals
  - Image processing and analysis
  - Fuzzy sets and systems, neuro-fuzzy systems
  - Pattern recognition
  - Cybernetics
  - Computer assisted medical diagnosis
  - Hospital information system
  - Picture archiving and communications systems
  - Medical information systems integration
  - Expert systems in medicine
  - Time-frequency analysis of biomedical signals
  - Multirate signal processing
  - Evolutionary computations
  - Artificial neural networks
  - Data mining
  - Artificial intelligence

- Design, construction and testing of electronic medical apparatus
  - Design and construction of amplifiers for biological signals and data acquisition systems co-operating with computers
  - Testing of electromedical apparatus
  - Design of electronic devices for data acquisition

Courses

- Electromedical Metrology
- X-ray and Nuclear Imaging
- Medical Information Systems
- Electromedical Equipment
- Pattern Recognition
- Principles of Knowledge Engineering
- Diagnostic Imaging Systems
- Biocybernetics
- Computers in Medicine
- Diagnostic Cardiological Systems
- Computer Aided Medical Diagnosis
- Materials Science and Principles of Construction of Electronic Equipment
- Probability Theory and Mathematical Statistics
- Numerical Methods
- Biomedical Information Processing

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

Head of Division: Prof. Ewaryst TKACZ, PhD, DSc

Research staff

Prof. Ewaryst TKACZ, PhD, DSc

Prof. Sławomir KOŃCZAK, PhD, DSc

Kazimierz DRABCZYK, PhD
Dariusz KOMOROWSKI, PhD
Paweł KOSTKA, PhD
Piotr KOWALIK, PhD
Zbigniew PRUSZOWSKI, PhD
Jerzy ULJANOW, PhD
Krzysztof WACZYŃSKI, PhD
Edyta WRÓBEL, PhD

Weronika IZYDORCZYK, MSc

PhD Students

Wojciech FILIPOWSKI, MSc
Artur GINTROWSKI, MSc

Research fields

- Biotechnology and bioinformatics
  - Analysis of gene expressions
  - Computer assisted medical diagnosis
  - Time-frequency analysis of biomedical signals
  - Multirate signal processing
  - Evolutionary computations
- Design of electronic devices for data acquisition
- Application of organosilicon compounds to the production of doped glasses for semiconductor technology
- Special hybrid circuits made in thick (thin) film technology
  - Hermetic sealing of hybrid circuits based on epoxy plastics
  - Manufacture and stability testing of resistance ladders based on pastes of Polish production
  - Vapour deposition of metallic layers applied to hybrid circuits
- Chemical compounds for thick- and thin-film sensors
- Solar cells and photovoltaic systems

Courses

- Materials Science and Principles of Construction of Electronic Equipment
- Electromedical Metrology
- Bionics
- Computers in Medicine
- Biotechnology in Medicine
- Computer Assisted Diagnostics in Medical Care
- Artificial Organs
- Microelectronics
- Physics of Microfabrication
- Electronic Devices, Semiconductor Structures and Circuits
- Sensors
- Principles of Electron Technology
- Semiconductor Devices
- Special Semiconductor Devices
- Thin-Film Technology
- Thick-Film Technology
- Design of Thick/Thin-Film Circuits
- Hybrid Circuit Technology
- Hermetic Sealing
- Solid-State Physics
- Physics
- Physics in Medicine

STATUTORY ACTIVITES OF THE INSTITUTE OF ELECTRONICS

PhD DEGREES CONFERRED ON STAFF MEMBERS AND PhD STUDENTS OF THE INSTITUTE OF ELECTRONICS

1. **Andrzej Dzikowski**, Logic functions decomposition based on utilisation of Binary Decision Diagrams, PhD advisor: prof. E. Hrynkiewicz, 9 May 2006
2. **Tomasz Rudnicki**, Test-pattern generator for delay faults, PhD advisor: prof. A. Hławiczka, 22 June 2006
3. **Robert Czerwiński**, State assignment of finite state machines for PAL-based programmable devices, PhD advisor: Dr. D. Kania (DSc), degree with honours, 10 July 2006
4. **Wojciech Więcławek**, The fuzzy edge following technique for 3D segmentation of certain anatomical structures in radiological images, PhD advisor: prof. E. Piętka, 04 September 2006
5. **Piotr Zarychta**, Location and three-dimensional visualization of the ligaments in the MR knee images on the basis of fuzzy logic, PhD advisor: prof. E. Piętka, 04 September 2006
6. **Marcin Kucharczyk**, Forward error correction in transmission systems with multitone modulation, PhD advisor: prof. J. Rutkowski, 13 November 2006

RESEARCH GRANTS

Research activities of the Institute of Electronics are mainly financed by the Ministry of Science and Higher Education within the frames of a general research programme:

- ***Development of new research areas in electronics, telecommunication and signal processing***

Apart from this, each division of the Institute carries out its own research in the following general areas, which are further subdivided into individual research projects:

Division of Electronics Fundamentals:

- *Electronic components, circuits and systems - development of measurement methods, analysis and synthesis*

Division of Digital and Microprocessor Systems:

- *Multiprocessor systems, application specific integrated circuits and programmable logic devices and systems - analysis, design and testing*

Division of Circuit and Signal Theory:

- *Computer-aided methods of analysis, synthesis and testing of electronic systems and their selected applications*

Division of Telecommunication:

- *Development of methods and applications of digital channel commutation and transmission of digital signals, theoretical and experimental methods of examination of bodies radiating and dissipating electromagnetic waves*

Division of Biomedical Electronics:

- *Acquisition and processing of biomedical information*

Division of Microelectronics and Biotechnology:

- *Application methods of microelectronic technologies and biotechnologies*

In total, fifty-four individual research projects were completed in 2006.

GRANTS AWARDED BY THE COMMISSION OF EUROPEAN COMMUNITIES

1. **Project idealist34 „Partner Search Support for participants in IST Priority by European network of NCP for IST under the 6th Framework Program (IDEALIST34)", Contract No 511355 of 10th November 2004, duration: June 2004 – May 2006 (subcontracted from the Institute of Fundamental Technological Research, Polish Academy of Sciences) (Dr. T. Grabowiecki)**

   The objective of Idealist34 was to simplify and facilitate the participation in the IST Priority of organisations of all types. A focus was on newcomers and in particular on SMEs, including New Member States (NMS) and Associated Candidate Countries (ACC), Russia and Belarus. This objective was achieved by:

• Delivering and supporting a partner search mechanism with two goals:

   1. to help consortia find project partners for specific proposals
   2. to help potential participants find consortia they could join.

- Offering Idealist partner search services during international EC conferences and information days.
- IST NCP network in order to facilitate coordination between European and National Initiatives by contributing to the realisation of the ERA.

  The project funded cooperation between the IST National Contact Points (NCPs) and their representatives allowing them to provide a much broader and improved service to support cooperation on European level. Idealist34 focused on project partner searches across the whole of Europe and represented 34 countries.

2. Project idealist-extend „Extension of idealist34 project (the partner search and NCP support network for participants in the IST Priority) to INCO Balkan and NIS countries", Contract No 15813 of 27 September 2005, duration: February 2005 - June 2006 (Dr. T. Grabowiecki)

In idealist-extend 9 organisations from 2 EU countries, 3 Western Balkan Countries and 4 Newly Independent States supported proposers in their participation in the IST Programme. The partners were IST (Information Society Technologies) NCPs (National Contact Points) or were working in close cooperation with IST NCPs. Idealist-extend cooperated closely with the project idealist34 (proposal no. 511355), approved in IST Call 2 and started in June 2004. Both projects covered together 41 countries in Europe and neighbour regions and extended the IST project partner search to International Co-operation (INCO) countries. Idealist-extend strengthened NCP related organisations, trained both NCP related organisations and potential proposers in IST related questions, identified experts for call evaluations and brought together institutions at Infodays and workshops.

Idealist-extend

- offered INCO an effective project partner search service by making use of the already existing idealist34 partner search mechanism, making it easy to contact organisations in any country in Europe
- spread information about the IST programme within the participating INCO countries. It has built up a comprehensive project Website and additionally national project Websites of all participating project partners. Electronic newsletter was another means to promptly pass on up to date information about the IST programme. A project flyer and an

information brochure gave an introduction into the project and the possibilities it offered.

- Helped finding IST experts in the participating INCO states. It has built up a database of experts and published the data on Internet. This measure increased the visibility of the IST constituency in the participating INCO states. It has brought transparency into the regional IST Research landscapes and so made it easier for western project Co-ordinators to identify potential partners. Idealist-extend encouraged experts to apply for IST proposal evaluations organised by the European Commission in Brussels. This experience facilitated the preparation of their proposals in the future.

Idealist-extend introduced new partners to the whole IST community, as it brought together institutions from 41 countries. Being a network of NCPs, idealist34 and idealist-extend provided the NCPs informal backup based on personal relations and pooled resources. Idealist-extend contributed to the forming of the ERA, as it facilitated the coordination of NCPs or organisations working on behalf of NCPs in the IST Programme and it formed a platform for future cooperation.

3. Project IST- World - Knowledge Base for RTD competencies in IST Contract No 015823, duration: April 2005 - October 2007 (Dr. T. Grabowiecki)

The objective of the project is to set up and populate an information portal with automatic services that helps to promote RTD competencies in specific fields of IST in the NMS and ACC and facilitate and foster the involvement of RTD actors in joint research activities. The portal contains information about RTD actors on the local, national and international (European) level, such as persons, research groups, organisations and projects, and their experience and expertise. Such a unified portal makes information accessible that is currently spread over a variety of national and European databases. It adds value compared to existing databases by providing a single point of access to information about RTD expertise in the IST field in the NMS/ACC, and by providing innovative data analysis and social networking functionalities.
The portal will stimulate *active involvement* of researchers, research groups and organizations by building active professional virtual communities, using existing models for community building and maintenance upgrading them by community identification and community monitoring services.

The target user groups are organisations from all countries looking for specific RTD competencies, organisations from NMS/ACC wishing to promote their own competencies, and service providers (such as consultancies or other support actions requiring a knowledge base for their work).
The portal overcomes the shortcomings of the existing on-line services by offering advanced analytical and prediction services and by joining knowledge mapping with social networks building. It supports partner search for IST proposals and commercial projects by providing the following functionalities:

1. **Information Repository:** information about partners, their resources, active projects and their expertise.
2. **Partner Finding Tool:** predicting the optimum consortia of partners based on their competences, experiences and trust.
3. **Social Network Identification:** analysis of the present research activities, actors, social networks and results visualized by different techniques.
4. **Forecasting/Prediction:** forecasting of RTD trends based on monitoring of current research initiatives, projects and achievements, and predicting possible future research themes based on automatically detected trends.
5. **Expertise Identification:** summarising and presenting different aspects of a person's complex expertise profile based on extraction of information from a potentially huge number of web search results.

The information portal and promotion activities focus on two out of four major thematic priorities within IST:

1. Knowledge and interface technologies

2. Applied IST research addressing major societal and economic challenges

The best coverage for the NMS/ACC is assured by importing or harvesting already existing data, and by promoting self-registration in the portal through multipliers in different countries, with special emphasis on SMEs. Organisations of all countries from NMS/ACC are represented in the consortium. Of course, the portal is not restricted to organisations from NMS/ACC, but it is open to experts and organisations from all of Europe.

4. MAPPER Project (Model-based Adaptive Product and Process Engineering), 6th Framework Programme of European Union) - FP6-2004-IST-NMP-2, Project 016527 (Dr. A. Pawlak)

During the first year of the project the group from the Institute of Electronics (SUT) cooperated with a number of MAPPER partners on project methodology, services, and a configurable platform (MAPPER infrastructure). The group worked especially closely with Evatronix SA company (Dr. Wojciech Sakowski) on definition of requirements on the MAPPER platform for integration of design services (deliverable D5 "IP-based SoC design requirements model"). The requirements that have been defined together with Evatronix address use of the mentioned configurable platform in design of electronic systems using IP-components. First Active Knowledge Models[1] of Evatronix design processes were developed in cooperation with the Norwegian company AKM. These requirements together with those from CRF (Fiat Research Centre, Orbassano) and Kongsberg Automotive (Swedish supplier of car accessories) were the basis for research on participatory design methodology (cooperation with Norwegian R&D centre SINTEF, FernUni Hagen, University of Trento, and Vienna University of Technology) that is formulated and supported by MAPPER. The defined requirements were also used in directing our R&D on the configurable platform, as well as on design and collaboration services to be developed during the remaining project time period (cooperation with AKM company, FernUni Hagen and Fraunhofer IGD Darmstadt).

Configurable design services defined and developed by the project use the "web services technology" as the underlying backbone. These services are being integrated with the main component of the platform, namely with the AKM platform for active knowledge models (e.g., enterprise, electronic system design, or a product in the automotive industry). In the frame of R&D on the project platform, our group develops services being a part of the new version of our TRMS system (*www.ecolleg.org/trms*).

As a partner responsible for exploitation and dissemination of project results our group co-organised the consultation workshop of the AITPL (Ambient Intelligence Technologies for the Product Lifecycle) cluster of projects on the AITPL themes in the 7th Framework Program of EU (Brussels, 27.02.2006). We also organised the CCE06 workshop on *Challenges in Collaborative Engineering* (*Prague, 19-20.04.2006, cce.ecolleg.org/2006/*).

[1] Information on active knowledge modelling is available on the AKM company web pages: http://www.activeknowledgemodeling.com/

The first public reports and other documents will be available soon from the MAPPER project portal *at mapper.eu.org.*

INDIVIDUAL RESEARCH GRANTS AWARDED BY THE MINISTRY OF SCIENCE AND HIGHER EDUCATION TO STAFF MEMBERS OF THE INSTITUTE

1. **Prof. E. Piętka,** Remotely accessible data base of standard radiograms for computer aided bone age assessment
2. **Prof. E. Tkacz**, Elaboration of A new methodology for non-invasive follow-up estimation in the case of patients with ischaemic brain stroke using both Heart Rate Variability (HRV) and Heart Rate Turbulence (HRT) analyses
3. **Prof. E. Tkacz,** Elaboration of the Emergency Lighting System with Central Monitoring and Control of Sockets and Emergency Devices in Case of Object Under Terrorist Attack Risk
4. **D. Kania (PhD, DSc)**, Logic synthesis of digital circuits for PAL-based CPLDs
5. **D. Grzechca (PhD),** Hardware Implementation of the Hybrid Methods to Analog Fault Circuits Diagnosis
6. **A. Noga (MSc),** (PhD grant, advisor: prof. A. Karwowski), Improvement of efficiency of the hybrid MM-PO method for wide-band analysis of radiating structures
7. **T. Topa MSc),** (PhD grant, advisor: prof. A. Karwowski), An effective hybrid method MoM-FDTD for wide-band analysis of radiating and scattering objects

INTERNATIONAL CO-OPERATION

1. Technical University of Ostrava, Department of Measurements and Control, Czech Republic (Prof. E. Hrynkiewicz)
2. University of Southern California (Prof. E. Piętka)
3. SECTRA – Sweden (Prof. E. Piętka)
4. Centre Nationale de Recherche Scientifique, Nancy, France (Dr. N. Henzel)
5. Linköping University, Sweden, (D.r J. Konopacki)
6. Technical University of Brno, Czech Republic (Prof. E. Tkacz)

SCIENTIFIC CONFERENCES ORGANISED AND CO-ORGANISED BY THE INSTITUTE OF ELECTRONICS

1. Programmable Devices and Systems (PDeS'06), IFAC Workshop, PDeS 2006, Brno, Czech Republic, 14 – 16 February 2006 (Prof. E. Hrynkiewicz)
2. Workshop on CHALLENGES IN COLLABORATIVE ENGINEERING (CCE'06) – The Integration Challenge in Industrial Collaborative Engineering, Prague, Czech Republic, 19-20 April 2006, in conjunction with DDECS'06 (general co-chair: Dr. A. Pawlak)
3. The Fifth International PhD Students' Workshop Control and Information Technology IWCIT 2006, Silesian University of Technology, Institute of Electronics, Gliwice, 21–22 September 2006 (Prof. Z. Filus)
4. International Conference Medical Informatics & Technologies (MIT), Wisła, Poland, 25-27 September 2006 (Prof. E. Piętka)

STAFF MEMBERS PARTICIPATING IN SCIENTIFIC AND ORGANISING COMMITTEES OF CONFERENCES AND SYMPOSIA

International

1. **Prof. Z. Filus**, Chairman, International PhD Students' Workshop Control and Information Technology IWCIT 2006, Silesian University of Technology, Institute of Electronics, Gliwice, 21–22 September 2006
2. **Prof. A. Hławiczka,** General chairman, the IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Brno, Czech Republic, 18-21 April 2006
3. **Prof. E. Hrynkiewicz,** Programmable Devices and Systems (PDeS'06), IFAC Workshop, PDeS 2006, Brno, Czech Republic, 14 – 16 February 2006
4. **Prof. E. Hrynkiewicz**, the IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS), Brno, Czech Republic, 18-21 April 2006
5. **Prof. E. Hrynkiewicz**, International PhD Students' Workshop Control and Information Technology IWCIT 2006, Gliwice, 21-22 September 2006

6. **Prof. E. Hrynkiewicz**, The 3rd IFAC Workshop on Dicrete-Event System Design (DESDes 2006), Rydzyna, Poland, 26-28 September 2006
7. **Prof. A. Karwowski**, Chairman, 18th International Wrocław Symposium and Exhibition on Electromagnetic Compatibility, Wrocław, 28-30 June 2006
8. **Prof. A. Karwowski**, member of the Programme Committee, 16th International Conference on Microwaves, Radar and Wireless Communications (MIKON 2006), 22-24 May 2006, Cracow
9. **Prof. A. Karwowski**, Programme Committee of the National Conference on Radiocommunication, Radiodiffusion and Television KKRRiT 2006, 7-9 June 2006
10. **Dr. A. Pawlak**, General co-chair and PC member, Workshop on Challenges in Collaborative Engineering CCE'06, Prague, April 19-20, 2006
11. **Dr. A. Pawlak**, DDECS 2006 – 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, Prague, April 19-20 2006
12. **Prof. E.Piętka**, Chairwoman, International Conference Medical Informatics & Technologies (MIT), Wisła, September 25-27, 2006
13. **Prof. E. Piętka**, member of the Programme Committee of Computer Assisted Radiology and Surgery
14. **Prof. E. Piętka**, member of the Programme Committee of European Congress of Radiology
15. **Prof. J. Łęski**, International Conference Medical Informatics & Technologies (MIT), Wisła, September 25-27, 2006
16. **Prof. E. Tkacz**, International Conference Medical Informatics & Technologies (MIT), Wisła, September 25-27, 2006
17. **Prof. J. Rutkowski**, International Conference on Signals and Electronic Systems ICSES, Łódź, September 17-20, 2006

National

1. **Prof. Z. Filus**, National Electronics Conference, Koszalin-Darłowo, 13-15 June 2006
2. **Prof. E. Hrynkiewicz**, National Conference Reprogrammable Digital Circuits RUC 2006, Szczecin, 18-19 May 2006

3. **Prof. E. Hrynkiewicz**, National Electronics Conference, Koszalin-Darłowo, 13-15 June 2006
4. **Prof. E. Hrynkiewicz**, Scientific Conference „Informatics – The Art or The Craft", Złotniki Lubańskie, Poland, 19-22 May 2006
5. **Prof. L. Lasek**, National Electronics Conference, Koszalin-Darłowo, 13-15 June 2006
6. **Prof. J. Rutkowski**, National Electronics Conference, Koszalin-Darłowo, 13-15 June 2006
7. **Prof. J. Rutkowski**, Conference "Computer Networks", Zakopane, 21-23 June 2006
8. **Prof. J. Rutkowski**, Databases: Applications and Systems, Ustroń 30 May – 2 June 2006

REVIEWERS

1. **Dr. R. Czabański**, Fuzzy Sets and Systems, IEE Proceedings Control Theory & Applications, International Journal of Applied Mathematics and Computer Science
2. **Prof. A. Hławiczka**, grant proposals for the Czech Grant Agency (since 2000)
3. **Prof. E. Hrynkiewicz,** grant proposals for the Czech Grant Agency (since 2000), International Journal on Applied Mathematics and Computer Science; Sensors, Annales UMCS – Informatica, IEEE - ICSES
4. **Prof. A. Karwowski,** IEE Proceedings Microwaves, Antennas & Propagation (London), Electronic Letters, IEEE Transactions on Antennas and Propagation, IEEE Transactions on Microwave Theory and Techniques, International Symposium and Exhibition on Electromagnetic Compatibility (EMC)
5. **Prof. J. Łęski**, Medical Science Monitor (papers on Medical Technology), IEEE Trans. Neural Networks, International Journal Applied Mathematics and Computer Sciences, IEEE Trans. Systems, Man & Cybernetics, Journal of Applied Computer Science, European Journal of Operational Research, Fuzzy Sets and Systems, Pattern Recognition Letters, IEEE Trans. Biomedical Engineering, IEEE Trans. Fuzzy Systems, Journal of Theoretical and Applied Mechanics, IEEE Trans. Signal Processing, Computational Statistics and Data

Analysis, Bulletin of the Polish Academy of Sciences, BioMedical Engineering OnLine, Pattern Analysis and Applications

6. **Prof. E. Piętka,** CARS – Computer Assisted Radiology and Surgery, EuroPACS (European PACS Society), CORES, IEEE Transactions on Medical Imaging, Computerised Medical Imaging and Graphics, Medical Science Monitor, European Journal of Operational Research, Modelling and Simulation in Engineering VLSI Design
7. **Prof. J. Rutkowski**, IEEE Transactions on Computer Aided Design (CAD)
8. **Dr. T. Garbolino,** reviewer of EU project proposals
9. **Dr. M. Kotas**, IEEE Transactions on Biomedical Engineering
10. **Dr. A. Pawlak**, reviewer of EU projects and project proposals
11. **Prof. E. Tkacz,** grant proposals for the Czech Grant Agency, IEEE Transactions on Biomedical Engineering; Elsevier Signal Processing

OTHER IMPORTANT AFFILIATIONS

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6. **Prof. E. Hrynkiewicz**, member of the Electronics and Telecommunication Committee, Polish Academy of Sciences
7. **Prof. E. Hrynkiewicz**, member of the section Electronics at the Ministry of Science and Higher Education

8. **Prof. E. Hrynkiewicz**, Chairman of the section Electronics at the Katowice Branch of the Polish Academy of Sciences
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11. **Prof. E. Hrynkiewicz**, Member of IFAC Technical Committee TC 4.1 on Components and Technologies for Control
12. **Prof. A. Karwowski**, founder and Chairman of the Polish Chapter of the IEEE Electromagnetic Compatibility Society
13. **Prof. A. Karwowski**, Vice-Chairman of the Antennas and Propagation Society, AP/AES/MTT Joint Chapter of the IEEE Poland Section
14. **Prof. A. Karwowski**, member of the 4th Workgroup (WG 4) "Characterization of high frequency electromagnetic fields and SAR produced by specific sources", Technical Committee 106 "Methods for the assessment of electric, magnetic and electromagnetic fields associated with human exposure" of the International Electrotechnical Commission (IEC)
15. **Prof. A. Karwowski,** member of the Project Team (PT) 62209 "Human Exposure to Radio Frequency Fields from Handheld and Body-Mounted Wireless Communication Devices - Human models, Instrumentation, and Procedures", Technical Committee 106, IEC
16. **Prof. A. Karwowski,** member of the Project Team (PT) 62232 "EM fields from base stations for mobile telephone", Technical Committee 106, IEC
17. **Prof. A. Karwowski,** member of the Technical Committee 104 for Electromagnetic Compatibility of the Polish Standardisation Committee
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24. **Prof. J. Łęski**, member of the Steering Committee at the Gliwice-Opole Branch of the Polish Society of Theoretical and Applied Electrotechnics
25. **Prof. J. Łęski**, member of the Scientific Committee of the Biomedical Engineering Centre
26. **Dr. A. Pawlak**, member of IFIP (International Federation for Information Processing) W.G. 10.5 "Electronic Systems Description and Design Tools"
27. **Dr. A. Pawlak**, correspondent of EUROMICRO Association
28. **Prof. E. Piętka,** IEEE Poland Section – Engineering in Medicine and Biology – chair of the EMS Chapter
29. **Prof. E. Piętka,** member of the Board of European PACS Society – EuroPACS
30. **Prof. E. Piętka,** National Committee for Collaboration with Committee on Data for Science and Technology (CODATA) at the Polish Academy of Sciences
31. **Prof. E. Piętka,** member of the Section Electronics at the Katowice Branch of the Polish Academy of Sciences
32. **Prof. J. Rutkowski**, member of the Evaluation Committee for Electronics and Telecommunication, Accreditation Commission for Technical Universities
33. **Prof. J. Rutkowski**, Section on Signals, Circuits and Systems of the Electronics and Telecommunication Committee, Polish Academy of Science
34. **Prof. E. Tkacz,** member of the International Advisory Board of the Annual Journal of Medical Informatics and Technology published by the University of Silesia
35. **Prof. E. Tkacz,** member of the Section Electronics at the Katowice Branch of the Polish Academy of Sciences

36. **Prof. E. Tkacz,** IEEE/EMBS (Engineering in Medicine and Biology Society)
37. **Prof. E. Tkacz,** EUROSIM – BIOSIGNAL, TTK (Polish Cardiac Society)
38. **Prof. E. Tkacz,** ECS (European Cardiac Society)

PATENTS

1. **Dr. Mirosław Magnuski**, Patent No. 192968, December 2006, „A method of measurement of amplitudes and phase shift of scattering waves, microwave vector voltmeter for measurement of amplitudes and phase shift of scattering waves"
2. **Dr. Andrzej Czapla†,** Patent No. 193655, September 2006, „A manipulator for the examination of tapping"
3. **Dr. Adam Kristof**, Patent application No. P-379604 of 4 May 2006, "A method of linearization and biasing and a structure of the final stage of a push-pull power amplifier"

OTHER IMPORTANT INFORMATION

In cooperation with Mentor Graphics Corporation, a course of Printed Circuit Board Design was carried out in 2006. The course, based on Mentor software tools, was focused on the design and putting into production sophisticated PCBs for modern digital and mixed AD electronic devices. 40 5th-year students from Electronics&Telecommunications and Macrofaculty at the Faculty of Automatic Control, Electronics and Computer Science have successfully completed the course.

LIBRARY RESOURCES OF THE INSTITUTE OF ELECTRONICS

Total number of book titles	9217
Total number of journals	1997
Number of subscribed national journals	11
Number of subscribed foreign journals	20

LIST OF PUBLICATIONS - 2006

The Institute publishes its own publication, Zeszyty Naukowe Pol. Śl. ELEKTRONIKA, edited by Asst. Prof. Zdzisław Pogoda. Fourteen issues have been published up to now.

1. Adamowicz B., **Izydorczyk W**., Klimasek A., **Waczyński K**., **Uljanow J**., Jakubik W., Żywicki J., Studies of chemical composition and response of the SnO_2 based sensor structure to dry and humid synthetic air, Elektronika No. 12/2006, SIGMA-NOT, pp. 5-6
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ABSTRACTS OF SELECTED RESEARCH PROJECTS

DIVISION OF ELECTRONICS FUNDAMENTALS

Prof. A. Karwowski, A. Noga (MSc), T. Topa (MSc), *Improving efficiency of hybrid Computational Electromagnetics Techniques*

This research aims at improving computational efficiency of two selected Computational Electromagnetic Techniques (CEM), namely, MoM–PO (Method-of-Moments–Physical Optics) and MoM–FDTD (Method-of-Moments–Finite Difference Time Domain). MM-PO performances have been investigated in the context of wide-band analysis of antennas radiating in close proximity of electrically large conducting bodies, and two methods of improving efficiency have been thoroughly examined: (1) applying the impedance matrix interpolation technique in the frequency domain, and (2) employing a dynamic adaptive frequency sampling of the desired observable. Both these methods are not basically new but combined together yield an extremely computationally efficient technique which seems to have a bit of novelty and offers spectacular saving in terms of both CPU time and memory storage relative to the conventional MM-PO and MM approaches.

In turn, MoM-FDTD hybrid approach requires the information to be exchanged forth and back between the MoM-regions and the FDTD-regions coupled through the Huygens surfaces. For electrically large structures, evaluation of the electric and magnetic field components and related equivalence-principle sources on the Huygens surfaces can represent a significant (even dominant) fraction of the total solution time required for the problem. Within this research, we have demonstrated a possibility of increasing computational efficiency of MoM-FDTD hybrid method by employing spatial interpolation combined with adaptive sampling in calculating the electric and magnetic field components and the effective sources on the Huygens surfaces. Numerical examples show that the proposed approach offers a considerable CPU time saving.

A. Malcher (PhD), *A self-calibrating converter of impedance components for capacitive sensors*

Impedance sensors are often used for analog to digital conversion of physical quantities. In these sensors two impedance components (e.g. capacitance and resistance) change according to the measured quantity. For the calculation of the measured quantity it is required to know both impedance components.

In this research work a new method of analog to digital conversion of impedance components has been developed. The circuit is intended for measuring impedance,

which can be represented as a capacitor and a resistor connected in series. The idea of this method is to use an oscillating structure in which the frequency depends on the capacitive component, while a particular DC control voltage depends on the resistive component. Resistance and capacitance of the sensor can be calculated as a result of frequency and DC voltage measurement.

Practically built circuits showed a significant nonlinearity and a noticeable interaction effect between the components. It was necessary to find approximation functions that made it possible to correct these nonlinearities and interactions. These functions contain four coefficients, so four-point calibration is required. In order to find them a computer controlled calibration circuit was built.

The conversion characteristics were measured and the errors were discussed. Some improvements were suggested.

The experimental results show that the capacitive part can be converted with the nonlinearity error less than 0.3% and with a very high resolution reaching 5 ppm. The nonlinearity of converting the resistive part is worse, namely about 3%.

Z. Rymarski (PhD), *PWM-AC signal quality in sinusoidal inverters and amplitude control in single-phase inverters*

The quality ratio of the output signal from an inverter should enable the characterization of the PWM modulator properties. Usually the THDV ratio of the load waveforms depends on the type of load and on the output filter parameters. The THDV ratio (or WTHDV) of the PWM-AC voltage signal used separately as the quality ratio can lead to false conclusions. Therefore it should be used simultaneously with another, "artificial" LHDV ratio, presenting the influence of the lowest harmonics of the modulating frequency, because THDV depends mainly on high order harmonics ($f_h > 0.5f_s$). LHDV ratio strongly depends on the frequency ratio (p) and the modulation depth (M), THDV ratio depends mainly on the modulation depth. The THDV/LHDV ratios pair allows for a characterization of the PWM-AC signal and foreseeing the distortions of the sinusoidal output signal for different kinds of PWM inverters. The THDV/LHDV pair gives objective information about the modulator and the power stage of the inverter. The analysis of the PWM-AC signal spectrum enables to determine the parameters of the output LC filter. The standard, 3-level single edge and the double edge regular modulators (that can model the operation of all other modulation techniques in a steady state) were compared using THDV/LHDV ratios. Clear results can be seen for the high enough ($p > 30$) frequency ratio. The breadboard verification – measuring the spectrum of the experimental inverter PWM output voltage confirms the theoretical considerations. Measurements show that some second order effects slightly increase the LHDV ratio. A high frequency ratio (p) ensures a sufficient quality of the inverter output signal for any type of modulation.

In inverters with an output transformer, the instantaneous control can disturb magnetizing current of the transformer, so the carrier waveform modulation is

preferred. The overmodulation in a single-phase inverter with an output transformer improves its dynamic properties when the output voltage amplitude is controlled. The overmodulation was previously presented as a method for increasing output voltage but was not analyzed as a method for improving transient response of the inverter. Lowering the transformer ratio n_2/n_1 and enabling the overmodulation (M>1) reduces the output impedance, but introduces low order harmonics and enlarges the error of measuring the amplitude. The overmodulation is a way to improve the transient response of the inverter with the output transformer. The static and dynamic errors of the output voltage amplitude control with hardware and software rectification were presented. The numbers of samples per modulating period for amplitude control methods were calculated. The method with hardware rectification requires a lower number of samples and it is synchronization error insensitive. The measured dynamic properties of the 700 VA inverter (M<120%, software rectification, internal synchronization, 128 samples and resistive load) are close to the simulated transient response.

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

Prof. E. Hrynkiewicz, M. Chmiel (PhD), A. Milik (PhD), *Programmable Logic Controllers – Architecture, Programming and Implementation*

The research work carried out in the domain of Programmable Logic Controllers (PLC) is concentrated on the development of a modified architecture of CPU and optimized program execution that are aimed at the reduction of response time.

Dual processor controller architecture is considered that consists of bit and byte processing units. Optimisation of the program execution process allows concurrent operation of both units. Hardware supported synchronization and task passing among processors simplifies development of the control program and possibly maintains the highest computing performance. Research carried out in the domain of program execution has proved that performance of logic controllers can be greatly improved by selective program execution. Research into the selective program execution is carried on. It is expected to obtain a completely new CPU architecture, dedicated for automatic control purposes, that is able to selectively execute program blocks.

In contrast to software implementation of control program, the research group also develops control algorithm implementation in digital reconfigurable processing units based on FPGA devices. Hardware implemented control algorithms are the fastest solution. Several architectures have been developed that allow constructing controllers with compact or modular architecture. Appropriate programmatic tools that allow for simple programming of control task have been developed and are continuously improved. Programming tools are oriented for optimized implementation of the developed control algorithms.

Recently dynamic reconfiguration has been one of the main fields of interest for the research group concerned. It is expected to be extremely useful in the domain of data processing.

Prof. E. Hrynkiewicz, A. Dzikowski (PhD), *BDD-based decompositions of multiple output logic functions*

As a result of research a modification of the method dedicated to a complex area decomposition of a set of logic functions has been elaborated. The modified method is dedicated to implement the considered logic circuits within FPGA structures. The authors attempted to reach solutions where the number of configurable logic blocks and the number of structural layers would be reasonably balanced on the basis of the minimization principle. The main advantage of the procedure when the decomposition is carried out directly on the BDD diagram is the opportunity of immediate checking whether the decomposed areas of the diagram do not exceed the resources of logic blocks incorporated into the integrated circuits that are used for implementation of the logic functions involved.

After having applied the method of decomposition directly on the BDD to a series of test functions the obtained results were compared with other results of logic synthesis as published in literature and the results of comparison were brought together in a table. The gathered information can provide good reasoning to state that satisfying results can be achieved for most circuits by means of the method of serial decomposition.

For such test functions as rd53, rd73 and rd84 the method of advanced decomposition with searching for adders quite frequently leads to much better solutions. To improve the quality of solutions as obtained by the method with searching for adders one can carry out modification of the eventual result, whereas the applied modification techniques are determined by the desired objective.

The objective of modification can be specified either unambiguously as minimization of the hardware (number of CLB modules) or reduction in the number of hierarchic layers (propagation time) or sometimes a compromise between both strategies can be reached. In many cases a detailed and thorough analysis of logic functions covered by individual CLB modules makes it possible to improve optimization of the final logic circuit.

Prof. A. Hławiczka, T.Garbolino (PhD), K. Gucwa (PhD), *Test-per-clock detection, localization and identification of interconnect faults*

A novel method for detection, localization and identification of faults in interconnects between IP (Intellectual Property) cores in SoC (System on Chip) has been presented. The method employs a compaction of test responses appearing at the outputs of NUT (network under test). Using a compactor allows for testing the interconnects test-per-clock method. The testing process was split into two phases. During the first phase a short test sequence, providing only detection of faults, is used that reduces the test time

for fault free circuits. During the second phase (that is performed only in the case of the detection of faults in the first phase) a long test sequence of full diagnostic resolution is used. During the last step the information stored in signatures is exploited. Because the signature is chosen to be 32 bits long, error aliasing is negligible. The proposed hardware concept is independent of the type of both the detection test sequence and the localization test sequence. The sequence must only provide stimulation of all tested faults. A classical MISR register based on the D-type flip-flop or MISR based on the T-type flip-flop can be used for implementation of the compactor. However, the authors proved in previous works that, if the NUT is stimulated with typical test sequences, the compactor using T-type flip-flops has lower error aliasing probability. During the first phase (detection phase) MISR is used for compaction of all responses at its inputs simultaneously. During the localization phase the MISR is converted into specific SISR that performs the compaction sequence appearing only at one chosen MISR input (other inputs are kept in the 0 state). In that case the signature obtained depends on the number of MISR input (being the SISR input), for that reason the authors introduced a new notion – the normalized signature. The normalized signature does not depend on the number of MISR/SISR input that is fed with the test sequence. It depends only on the sequence applied. A way of calculation of the normalized signature based on the signature obtained in MISR was given. Using the normalized signature substantially simplifies the process of fault localization and identification. Moreover, the authors propose to test the testing hardware itself, what makes the results reliable.

D. Kania (PhD, DSc), A. Milik (PhD), R. Czerwiński (PhD), J. Kulisz PhD), *Synthesis strategies dedicated for PAL-based CPLD circuits*

A characteristic feature of most contemporary CPLD circuits is their structure, which consists of PAL-like building blocks, containing a limited (and small, e. g. 3, 4, 5) number of product terms. Implementation of functions in logic blocks of that kind usually requires partitioning - i.e. decomposition of the function into logic blocks requiring smaller numbers of products. Most of contemporary commercial tools supporting CPLD design are based on the so called *Classical Method*, which leads to implementations in the form of a multi-level structure with cascaded feedback connections between the PAL-like blocks.

As a result of the research project two new synthesis methods, dedicated for PAL-based CPLDs, have been developed. Both methods are based on function decomposition. The first method is dedicated for multiple-output functions. The algorithm is based on the classical Curtis approach. The essence of the method consists in searching for a partitioning of the designed circuit into subcircuits of similar complexity. An important feature of the method is uniform usage of product terms available in the PAL-blocks, which is achieved by using the so-called *Homogenous Coding*.

The second of the methods - the *Row Decomposition* method - is dedicated for single-output functions. The essence of the method consists in searching for a partitioning of input variables, which provides feasibility of implementation of the free block in one

PAL-based block. The key problem in the appropriate decomposition search is determining the so-called *Row Complexity* of the partition matrix. For this purpose a new concept of graph - the *Row Incompatibility and Complement Graph* - has been proposed.

During the research work a few new synthesis algorithms dedicated for FSM-s have also been developed. The key feature of the algorithms is efficient usage of product terms available in PAL-based blocks, which was achieved by anticipating effects of two-level minimisation, and technology mapping, already during internal state coding. The methods are based on some new concepts, i.e. analysis of *Primary* and *Secondary Merging Conditions*, and the *Implicant Distribution Table*.

The methods developed were verified using the standard set of benchmark functions. The results of the experiments show that the new algorithms are much more effective than the classical method both with respect to the number of logic block used, and the number of logic levels.

A. Pawlak (PhD), D. Stachańczyk (PhD). M. Ślęzak (PhD), P. Penkala (MSc), M. Witczyński (MSc), P. Fraś (MSc), *Colaborative Engineering in Electronics*

Collaborative engineering (CE) is a new Internet-based approach to engineering. A research group dealing with CE challenges was established in the Institute of Electronics in the year 2000 in order to fulfil tasks of the first acquired European 5FP E-Colleg project (*www.ecolleg.org*). The topic of distributed collaborative work was extended with an organisational perspective due to the follow-up VOSTER project (*voster.vtt.fi*) (cluster of EU projects addressing issues of virtual organisations), and with visual knowledge-based approach due to the recently commenced 6FP MAPPER project (*mapper.eu.org*). Collaborative engineering in networks of cooperating (virtual) organisations is considered by us as enabling technologies for distributed collaborative design of electronic systems, and especially for IP-based System-on-a-Chip (SoC) design.

MAPPER related R&D tasks were in the centre of activities of the CE group in 2006. Among our main results we identify:

- definition of requirements on the MAPPER platform for integration of design services,
- further development of the TRMS (Tool Registration and Management Services) environment.

In cooperation with Evatronix SA an IP-based SoC design requirements model has been defined using the Active Knowledge Modelling (*www.activeknowledgemodeling.com/*) technology. The requirements address use of the mentioned configurable platform in the design of electronic systems using IP-components.

Configurable design services use the "web services technology" as the underlying backbone. These services are being integrated with the AKM platform for active knowledge models. In the frame of R&D on the project platform, our group develops services being a part of the new version of our TRMS system (*www.ecolleg.org/trms*).

We have also been active in the AITPL (Ambient Intelligence Technologies for the Product Lifecycle) cluster of projects (*www.ve-forum.org/apps/pub.asp?Q=1271*) and organised the CCE06 workshop on *Challenges in Collaborative Engineering* (Prague, 19-20 April 2006, *cce.ecolleg.org/2006/*).

DIVISION OF CIRCUIT AND SIGNAL THEORY

J. Dąbrowski (PhD, DSc), J. Konopacki (PhD), *An SC filter for RF sampling and downconversion with wideband image rejection*

With an increasing number of standards used around the world today there is an enormous need for low cost multistandard RF front-ends. The traditional view of software defined radio (SDR), where the analog-to-digital converter (ADC) is placed directly at the antenna or after the low-noise amplifier (LNA), puts unrealistic requirements on the ADC in terms of sampling rate and resolution resulting in too high power consumption. The key to success is to have an RF front-end architecture that is highly flexible without putting too tough requirements on the ADC. One approach to do this is the RF-sampling front-end. The basic idea is to sample the RF signal after the LNA and do further processing and necessary decimation before AD conversion. Today's CMOS technologies demonstrate very high speeds, making the RF sampling technique appealing in a context of multistandard operation at GHz frequencies. The problem of RF sampling and downconversion has already been discussed in the literature. However, more efficient image suppression is considered in the project, especially useful for wideband signals, such as those of the Wi-Fi WLAN standards operating in the 2.4 GHz band.

As for any receiver, the image problem appears critical. Basically, a good approach to avoid this problem is to use the zero-IF architecture. The design of a zero-IF receiver front-end, which adopts an RF sampling approach, is addressed in this project. To enable analog-to-digital conversion the sampled signal has to be decimated and band-limited. The decimation process introduces new image bands and an appropriate band-selection filter to remove these must be included. The concept of the sampling down-conversion filter incorporating decimation is derived. The prototype filter model is digital. It scales with frequency and provides efficient image suppression for a wide RF input range. An SC implementation of the circuit is discussed in detail. Simulations have been performed to validate this design.

The work was done in collaboration with the Linköping University (Sweden).

Prof. J. Rutkowski, T. Golonek (PhD), D. Grzechca (PhD), Ł. Chruszczyk (MSc), *The use of artificial intelligence methods for designing and diagnosing analog electronic circuits*

The current research project utilizes artificial intelligence methods to analog fault diagnosis. Due to tolerance dispersion of all elements in analog electronic circuits (AEC), distinguishing between healthy and faulty circuits is complex. Moreover, even a linear circuit with respect to the tolerance margin produces overlapping output nonlinear functions that are inseparable in the case of classical methods.

The most popular classical approach, based on mean square error measure, cannot distinguish all faulty and healthy circuits. One of the weakest points of the method is the size of dictionary that consists of thousands of patterns and even then, the level of fault diagnosis is not satisfactory. Therefore a few new techniques have been developed. A Neural Network (NN) as a classifier is the first method main core. Well-known generalization ability of the NN allows increasing classification ratio and reducing size of analog fault dictionary. Another advantage of the method is time domain testing procedure which takes into account three parameters: delay time, overshooting, and rise time. These features are fuzzyfied and feed NN afterwards. The fuzzyfication normalizes selected features by converting them into zero – one range which helps and increases NN convergence.

The second technique is related to analog test stimuli selection. A minimal set of sinusoidal excitations is constructed evolutionarily with the use of entropy index. This approach allows to maximize information reached from a circuit under test (CUT) and to minimize the number of necessary test measurements. The described method makes a decision about CUT diagnose after RMS or complex voltage measurements and its classifications to the adequate ambiguity sets (AS) for the selected frequencies. The widths of AS are determined adequately to the design tolerances of the CUT that assure protection before fault masking.

The third developed method combined approach to testing of analog electronic circuits by means of evolutionary algorithms, information theory and wavelet analysis. The testing procedure uses specialized aperiodic excitation that maximizes probability of fault detection and location. The testing method belongs to SBT (Simulation Before Test) class of fault diagnosis procedures and focuses on the most difficult case where very few (usually only input and output) nodes of the integrated circuit under test (CUT) are available.

DIVISION OF TELECOMMUNICATION

A. Dustor (PhD), *Biometric systems for identity verification*

Biometric systems for identity verification are based on physical or behavioral features of the human body, e.g. fingerprints, retina, iris, voice, hand geometry. Some of these features like iris ensure very high security at the cost of high false rejection probability

of a valid user by the system. Behavioral biometrics like voice changes with time and as a result voice verification has a relatively high error rate. Nowadays voice may be used only as an additional security level that is always combined with traditional security systems based on knowledge (password) or possession (code card, key). Nevertheless, speaker verification is very interesting to develop since this is the only biometrics that enables remote, via a telephone line, verification.

The aim of this work was to develop new speaker recognition techniques, more reliable than traditional methods based on Gaussian mixtures GMM and vector quantization VQ. As a result new classifiers, applying the Ho-Kashyap algorithm, were obtained. In these classifiers a nonlinear decision function is a superposition of several linear decision functions. Kernel functions and fuzzy systems were also applied. All developed classifiers have good generalization properties and yield lower error rates than the classical techniques.

P. Kłosowski (PhD), *Distance Learning Platform at the Silesian University of Technology*

Division of Telecommunication, which is a part of the Institute of Electronics, Silesian University of Technology, has specialized in advanced fields of telecommunication engineering for many years. One of them is e-learning, distance learning using the worldwide area network - Internet. The main research area in this field is Distance Learning Platform as e-learning service for all faculties of the Silesian University of Technology. Currently, over 400 online courses, created for students from twelve faculties of the University, are available on Distance Learning Platform. The number of Distance Learning Platform users exceeds 12000.

Distance Learning Platform is based on a modular object-oriented dynamic learning environment and it represents LMS (Learning Management Systems) technology, a software package designed to help educators create quality online courses. Such e-learning systems are sometimes also called Learning Management Systems (LMS), Virtual Learning Environments (VLE), education via computer-mediated communication (CMC) or Online Education. Distance Learning Platform runs without modification on Unix, Linux, FreeBSD, Windows, Mac OS X, NetWare and any other systems that support PHP, including most webhost providers. Data is stored in a single database: MySQL and PostgreSQL are best supported, but it can also be used with others.

Distance Learning Platform works as typically asynchronous e-learning service, but in the future more synchronous e-learning services will be added. Distance Learning Platform has a great potential to create a successful e-learning experience by providing a plethora of excellent tools that can be used to enhance conventional classroom instruction, in hybrid courses, or any distance learning arrangements.

M. Kucharczyk (PhD), *Forward error correction in transmission systems with multitone modulation*

This work presents different Forward Error Correction (FEC) coding schemes that can be used in a transmission system with Orthogonal Frequency Division Multiplexing (OFDM) modulation. OFDM is resistant to many signal distortions like intersymbol interferences and impulse disturbances, so it can be used for data transmission in such distorted environments as power lines. Redundant data encoding is required in such environments to achieve reliable communication, especially when SNR goes down over a longer distance.

Now the most popular FEC systems used with OFDM modulation are: convolutional codes, Reed-Solomon codes or both types of codes together (concatenated). These coding schemes and LDPC (Low Density Parity Check) codes are compared in this work. The length of the LDPC code word is equal to the length of the OFDM symbol in the presented system. Next modifications for the OFDM transmission system with an LDPC encoded/decoder were described:

The Iterative Sum-Product Algorithm (SPA) decoder for the LDPC code was connected by feedback with a frequency domain equalizer (FEQ) in the OFDM demodulator. Information from the decoder was used to increase precision of equalizer coefficients computation. As a result, BER (Bit Error Rate) of the whole system was decreased.

A lower BER and a particularly lower SER (Symbol Error Rate) were achieved using the genetic algorithm in the LDPC decoder. A syndrome with a low weight was often a result of the SPA algorithm. Then in a backward process the most probably falsified bits were found and using the evolutionary strategy the code word was searched, although sometimes not successfully found.

A proposal of using the presented algorithms in systems with a nonstationary channel was also put forward in this work.

DIVISION OF BIOMEDICAL ELECTRONICS

R. Czabański (PhD), *Fuzzy rules extraction using deterministic annealing integrated with ε-insensitive learning*

A fundamental problem while designing fuzzy systems is the determination of their rule base. Because there is no standard method of expert knowledge acquisition in the process of determining fuzzy if-then rules, automatic methods of rules generation are intensively investigated. A set of fuzzy conditional statements may be obtained automatically from numerical data describing the input/output system characteristic. A number of fuzzy rules extraction procedures use learning capabilities of artificial neural networks to solve this task. The integration of neural networks and fuzzy models leads to the so-called neuro-fuzzy systems. In this work a new method of fuzzy if-then rules

extraction using the ANBLIR (Artificial neural Network Based on Logical Interpretation of fuzzy if-then Rules) neuro-fuzzy system is presented.

ANBLIR is a computationally effective system with parameterized consequents based on both conjunctive and logical interpretations of fuzzy rules. It can be successfully applied to solve many practical problems such as classification, control, digital channel equalization, pattern recognition, prediction, signal compression and system identification. Its original learning procedure uses a combination of the steepest descent optimization and the least squares method. However, it may produce a local minimum in the case of a multimodal criterion function. The novelty of the learning algorithm consists in the application of a deterministic annealing method integrated with ε-insensitive learning. In order to decrease the computational burden of the learning procedure, a deterministic annealing method with a "freezing" phase and ε-insensitive learning by solving a system of linear inequalities are applied. This method yields an improvement of neuro-fuzzy modeling quality in the sense of an increase of generalization ability and outliers robustness. The advantages offered by the proposed algorithm are illustrated with two examples of its application concerning benchmark problems of identification and prediction.

Tomasz PRZYBYŁA (PhD), *The fuzzy myriad clustering method*

The clustering aims at assigning a set of objects to clusters in such a way that objects within the same cluster have a high degree of similarity, while objects belonging to different clusters are dissimilar. The clustering methods can be divided into hierarchical and nonhierarchical (partitioning) methods. In our investigation, clustering by minimization of the criterion function is considered. The most traditional clustering methods are "hard" partitioning i.e. every object belongs to one group. Such a kind of partition finds sharp boundaries among clusters. However, in practice, the boundaries are not strict but ambiguous. Thus soft partitioning is more suitable in this case. Fortunately, the fuzzy set theory proposed by Zadeh allows describing soft partitioning. The most popular method of fuzzy clustering is the fuzzy c-means (FCM) method proposed by Bezdek. The main disadvantage of the FCM method is its sensitivity to presence of outliers and noise in clustered data. In real applications, the data are corrupted by noise and assumed models such a Gaussian distribution are never exact. The FCM method is a prototype-based method, where the prototypes are weighted (fuzzy) means. The performance of linear estimation of prototypes is optimal for the Gaussian model of data statistics. The Gaussian model is inadequate in an impulsive environment. Impulsive signals are more accurately modeled by distributions whose density functions have heavier tails than the Gaussian distribution. The alpha-stable distribution can be a very good model for a wide range of impulsive environments and is a generalization of the Gaussian distribution.

The proposed prototype estimation method as weighted (fuzzy) myriad is derived from Maximum-Likelihood location estimators such as linear and weighted median estimators.

Some numerical experiments have been performed and the results are more accurate than the reference method outputs. So, the methods whose results are intuitively correct (the same or very similar to those expected) are worth being searched for.

W. Więcławek (PhD), *A 3D image analysis in segmentation of selected anatomical structures*

Image segmentation, resulting in an extraction of anatomical structures, is a crucial phase in image processing procedures. Being performed automatically, it is often problem-dependent and features poor precision. On the other hand, a manual approach may yield better results, yet is very time-consuming. In this approach a hybrid method has been implemented. It is based on the Live Wire method, yet has been significantly improved in terms of segmentation quality and numerical complexity.

The Live Wire algorithm (also known as Intelligent Scissors) defines the boundary detection process as an optimal path search in a weighted graph that represents the segmented image. In the conventional approach the gradient methods are employed. In this approach the wavelet decomposition has been implemented. The wavelet module and angle describe an edge pixel. It improves significantly the segmentation accuracy.

An optimal path searching method implements the Dijkstra algorithm. Unfortunately, numerical complexity is proportional to the image size. On the other hand, only pixels located next to the image edges are essential, while pixels within the homogeneous regions may not be considered. At this stage the fuzzy c-means method has been employed in order to reduce the image area to be subjected to the path searching algorithm.

The 2D algorithm has been extended to three dimensions. The fuzzy c-means procedure extracts the homogeneous region in the neighbour slice and morphological operations adjusted the edges. This methodology leads to 3D extraction of various anatomical structures including lungs, brain region, knee joints and may be implemented as the first step in a detailed region analysis.

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

P. Kowalik (PhD), Z. Pruszowski (PhD), *Thermoelectric force in Ni-P resistive layers*

Thermo-electric force is a phenomenon known for a long time. The first attempt of using the industrial thermo-electric effect took place in the 1960s of the last century. The main applications of thermoelectric effect are:

- thermoelectric generators,
- thermoelectric cooling modules.

Apart from using the thermoelectric force in the mentioned devices, it can be also a source of interferences in electronic devices. This mainly takes place in precise measuring devices, amplifiers and in other devices that deal with the heat emission effect, and what follows with existence of local temperature gradients.

The aim of this investigation was determining the thermoelectric force in high-precision resistors, with power dissipation factor up to 0.5 W and produced with amorphous Ni-P resistive layers.

P. Kowalik (PhD), Z. Pruszowski (PhD), *Fabrication of Co-P resistive layers by the chemical method*

In the production of precise resistors the following methods are usually used:

- cathode sputtering method based on deposition of material struck with high energetic ions from the cathode target,
- vapour deposition method based on deposition of the evaporated material on the substrates,
- chemical electroless plating method based on deposition of material from an aqueous solution on activated substrates. This method allows for deposition of alloys of about 30 elements, metals and non-metals.

So far, the electronics have used Ni-P alloys to produce fixed film resistors. The following investigation is pioneering because, so far, Co-P alloys have been used to produce magnetic layers.

W. Filipowski (MSc), K. Waczyński (PhD), K. Drabczyk (PhD), *Research on the preparation of spin-on glass solutions enabling the fabrication of highly doped silicon diffusion layers*

The market of solar cells is one of the most dynamic branches of modern silicon technologies. Unfortunately, the price of a cell is still a critical factor despite all the developments made recently. Nowadays, when the demand for cells is on the increase, most researches focus on the reduction in production costs trying to maintain the good quality of the cells produced. One of the basic elements of a multicrystalline silicon PV cell is the p-n junction. The area diffused in a wafer is the emitter layer which is formed during the diffusion doping of silicon which means that the process constitutes one of the key technological operations carried out during the production of PV cells. At present, diffusions are normally conducted in classical diffusion furnaces using classical dopant sources. As far as the fabrication of PV cells is concerned, cheap and fast doping technologies are being looked for and developed. The reduction in costs mentioned above may be obtained applying inexpensive and efficient dopant sources. Glaze prepared from alcohol, TEOS and orthophosphoric acid seems to be an interesting alternative. Apart from the classical technique of dopant application i.e. spinning, spraying may be used as well. Diffusion processes carried out in IR belt furnaces are a

promising solution since they enable fast diffusions and, more importantly, allow wafers of any size. Therefore, investigations into glaze as a dopant source, which may be easily used during the diffusions in IR belt furnaces, are being conducted.