Silesian University of Technology
Faculty of Automatic Control, Electronics and Computer Science

Annual Review 2009

Institute of Electronics

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Edited by
Maria Drelichowska

Institute of Electronics, March 2010

FOREWORD

The Institute of Electronics is a part of the Faculty of Automatic Control, Electronics and Computer Science, one of the 12 faculties of the Silesian University of Technology, founded in 1945. The University is located in Gliwice and has about 32,000 students at present. The Faculty of Automatic Control was founded in 1964, and after a few reorganisations it changed its name to the Faculty of Automatic Control, Electronics and Computer Science. Since its creation in 1974 the Institute of Electronics has been involved in various research and teaching activities. The Institute has about 100 members of academic staff and consists of six divisions:

- ***Division of Electronics Fundamentals and Radio Engineering***
- ***Division of Digital and Microprocessor Systems***
- ***Division of Circuit and Signal Theory***
- ***Division of Telecommunication***
- ***Division of Biomedical Electronics***
- ***Division of Microelectronics and Biotechnology***

The Institute specialises in such advanced fields of engineering as analogue and digital electronic systems, including biomedical systems, production of telecommunication and electronic systems etc. Research in these areas ranges from component to system level, encompassing practical and theoretical investigations with the application of both hardware and software techniques. Research groups are supported by a wide range of test and instrumentation equipment together with computer facilities, which can run with programming languages of all levels and offer various application software. Many of the Institute's research programmes are carried out in close co-operation with industry in order to satisfy the needs of the region, which is the main industrial centre of Poland.

The Institute offers 3.5-year courses leading to the degree of BSc and 1.5-year MSc courses. Both degrees are obtained on the basis of a project and a report, presented during a final examination. Since 2007 two-stage courses in Biomedical Engineering have also been run. The Institute participates in addition in a five-year MSc course in Automatic Control, Electronics and Computer Science, run by the Faculty, in which all teaching is in the English language. In 2007 this course was changed to the two-stage form too. The courses normally consist of lectures, laboratories, seminars and projects, and are followed by examinations. Apart from this, the Institute offers four-year courses at evening studies, leading to the degree of BSc. The curricula of the courses run by the Institute are designed for people who want to achieve both theoretical knowledge and practical skills in electronics. At present, the total amount of students is about 800. Other didactic activities include postgraduate and PhD studies.

The following pages provide detailed information regarding the research carried out as well as the subjects taught in each division.

CONTENTS

DIRECTORS OF THE INSTITUTE

Director of the Institute:

Prof. Edward HRYNKIEWICZ

Vice Director of the Institute for Research:

Prof. Zdzisław FILUS

Vice Director of the Institute for Teaching:

Asst. Prof. Adam BŁASZKOWSKI
(until August 2009)
Dr. Jacek KONOPACKI
(since September 2009)

DIVISION OF ELECTRONICS FUNDAMENTALS AND RADIO ENGINEERING

Head of Division: Prof. Zdzisław Filus, PhD, DSc

Research staff

Prof. Zdzisław FILUS, PhD, DSc

Prof. Andrzej KARWOWSKI, PhD, DSc
Prof. Leon LASEK, PhD, DSc
Asst. Prof. Adam BŁASZKOWSKI, PhD
Asst. Prof. Władysław CIĄŻYŃSKI, PhD
Andrzej BŁONAROWICZ, PhD
Jacek CHĘCIŃSKI, PhD
Jerzy FIOŁKA, PhD
Zenon KIDOŃ, PhD
Adam KRISTOF, PhD
Sławomir LASOTA, PhD
Mirosław MAGNUSKI, PhD
Andrzej MALCHER, PhD
Artur NOGA, PhD
Wojciech OLIWA, PhD
Zbigniew RYMARSKI, PhD
Maciej SURMA, PhD
Włodzimierz SZMELCER, PhD
Tomasz TOPA, PhD
Grzegorz WIECZOREK, PhD
Dariusz WÓJCIK, PhD
Piotr ZASTAWNIK, MSc

PhD Students

Przemysław POPOWICZ, MSc
Piotr FALKOWSKI, MSc

Research fields

- Electronic circuits synthesis
- Symbolic methods of electronic circuits analysis
- Electronic circuits for automotive applications
- Power electronic circuits
- Microprocessor-based measurement systems
- Computational electromagnetics
- Numerical modelling of radiating and scattering wire objects
- Linear antenna theory
- Electromagnetic compatibility
- Optoelectronics, Fiberoptics

Courses

- Semiconductor Devices
- Analogue Electronic Circuits
- Analogue Circuits Design
- Electronic Measurement Techniques
- Switching Circuits
- Special Semiconductor Devices and Circuits
- Materials Technology and Electronic Equipment Design
- Field and Wave Electromagnetics
- Introduction to Radiocommunication
- Radio Engineering Systems
- Fields, Waves and Antennas
- Wireless Computer Networks
- Design of Radio Electronic Devices
- High-Frequency Engineering Fundamentals
- Electromagnetic Compatibility

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

Head of Division: Prof. Edward HRYNKIEWICZ, PhD, DSc

Research staff

Prof. Edward HRYNKIEWICZ, PhD, DSc

Prof. Andrzej HŁAWICZKA, PhD, DSc
Asst. Prof. Zdzisław POGODA, PhD
Mirosław CHMIEL, PhD
Robert CZERWIŃSKI, PhD
Tomasz GARBOLINO, PhD
Krzysztof GUCWA, PhD
Eugeniusz KOSEK, PhD
Józef KULISZ, PhD
Adam MILIK, PhD
Adam PAWLAK, PhD
Krzysztof PUCHER, PhD
Tomasz RUDNICKI, PhD
Wojciech SAKOWSKI, PhD
Dariusz STACHAŃCZYK, PhD
Krzysztof TABOREK, PhD
Bernard WYRWOŁ, PhD
Dariusz POLOK, MSc

PhD Students

Jan MOCHA, MSc
Danuta PAMUŁA, MSc
Jakub MURAWSKI, MSc
Paweł SZWARC, MSc

Research fields

- Testing and testability of digital systems
  - Generation of test patterns
  - I_{DDQ} testing
  - Design for testability
  - Built-in self-tests and concurrent testing
  - Pseudorandom techniques for built-in tests for VLSI circuits and design of standard P1149 compatible chips
  - Microcomputer signature analysis
- Design of systems with CPLDs, FPGAs and programmable controllers
  - Design of support software
  - Logic synthesis
  - Implementation of logic structures in CPLDs, FPGAs and PSoCs

    - Fast operating CPU structures of programmable controllers and methods of PLC programming
    - Distributed structures of PLCs
    - PLC applications
    - Embedded control system design
- Frequency multipliers based on digital techniques
- Laboratory and industrial data acquisition and control systems
    - Signal conditioning
    - Analogue-to-digital and digital-to-analogue converters with optical isolation and fibre optic transmission systems
- Multiprocessor systems
    - Pipelining and parallel processing
    - Systems with global memory and arbitration
    - Statistical analysis of performance for pipelining processing
- ASIC design
    - High level design methodologies
    - System modelling and simulation (using VHDL and Verilog)
    - IP-core design
    - Distributed design methodologies based on Internet

Courses

- Digital Systems Fundamentals
- Design of Digital Devices
- Microprocessors Fundamentals
- Microprocessor Systems
- Reliability and Testing of Electronic Devices
- Computer Aided Design of Integrated Circuits
- Programmable Logic Devices
- Programmable Controllers

DIVISION OF CIRCUIT AND SIGNAL THEORY

Head of Division: Prof. Jerzy RUTKOWSKI, PhD, DSc

Research staff

Prof. Jerzy RUTKOWSKI, PhD, DSc

Tomasz GOLONEK, PhD
Tadeusz GRABOWIECKI, PhD
Damian GRZECHCA, PhD
Jacek KONOPACKI, PhD
Jan MACHNIEWSKI, PhD
Katarzyna MOŚCIŃSKA, PhD
Andrzej PUŁKA, PhD
Łukasz CHRUSZCZYK, PhD
Piotr JANTOS, PhD

PhD Students

Piotr KYZIOŁ, MSc

Research fields

- Computer-aided electronic circuits analysis and design
  - Failure diagnostics in analogue electronic circuits
  - Application of sensitivity methods to the analysis and synthesis of electronic circuits
  - Modelling and simulation of digital and mixed analog-digital circuits in VHDL language
  - System level design in SystemC
  - Application of artificial intelligence methods and genetic algorithms to circuit theory and electronics
  - Common-sense reasoning modelling and application of AI techniques to circuits models generation and verification
- Digital signal processing focused on digital filters design and application
- Signal processing and basic research into neural networks (analysis, synthesis and optimisation) and their application to engineering practice
  - Application of neural networks to image processing and recognition, including texture images
  - Application of wavelet techniques to signal processing
- Web – based education

Courses

- Circuit Theory
- Signal Theory
- Fundamentals of Electrical Engineering
- Information Theory and Coding
- Computer-Aided Design of Electronic Circuits
- Digital Signal Processing
- Biomedical Digital Signal Processing
- Neural Networks

DIVISION OF TELECOMMUNICATION

Head of Division: Dr. Jacek IZYDORCZYK

Research staff

Jacek IZYDORCZYK, PhD

Prof. Dariusz KANIA, PhD, DSc
Adam DUSTOR, PhD
Maria DZICZKOWSKA, PhD
Leszek DZICZKOWSKI, PhD
Grzegorz DZIWOKI, PhD
Piotr KŁOSOWSKI, PhD
Marcin KUCHARCZYK, PhD
Andrzej KUKIEŁKA, PhD
Wojciech SUŁEK, PhD
Jerzy WOJTUSZEK, PhD
Piotr ZAWADZKI, PhD

PhD Students
Mariusz BĄK, MSc

Research fields

- Digital commutation in modern telecommunication systems
  - Construction of telephone exchanges
  - Supervisory software for telephone exchanges
  - Special services (e.g. teleconferences)
  - Implementation of digital networks with integrated services (ISDN, B-ISDN, ATM)
- Application of digital signal processing to telecommunication
  - Compression of speech signal with the application of DSPs
  - Speech synthesis
  - Speech and speaker recognition
  - Application of artificial neural networks to signal processing
  - Design, testing and implementation of error correcting and modulating codes
  - Design of modern local area networks
  - Implementation and testing of new services in the Internet
  - xDSL technology

- Electromagnetic field engineering
  - Radiation and scattering of electromagnetic waves
  - Lightning protection
- Modems

Courses

- Fundamentals of Analogue and Digital Communication
- Fundamentals of Commutation
- Switching Nodes and Exchanges
- Principles of Transmission
- Communication Systems
- Signal Theory
- Information Theory and Coding
- Digital Signal Processing
- Computer-Aided Analysis of Electronic Circuits
- Digital Signal Processors (DSP)
- Neural Networks
- Computer Networks
- Internet
- Modems
- Introduction to Cryptography

DIVISION OF BIOMEDICAL ELECTRONICS

Head of Division: Prof. Jacek ŁĘSKI, PhD, DSc

Research staff

Prof. Jacek ŁĘSKI, PhD, DSc

Prof. Ewa PIĘTKA, PhD, DSc
Paweł BADURA, PhD
Robert CZABAŃSKI, PhD
Norbert HENZEL, PhD
Jerzy IHNATOWICZ, PhD
Jacek KAWA, PhD
Marian KOTAS, PhD
Tomasz PANDER, PhD
Stanisław PIETRASZEK, PhD
Sylwia POŚPIECH-KURKOWSKA, PhD
Tomasz PRZYBYŁA, PhD
Dominik SPINCZYK, PhD
Ewa STRASZECKA, PhD
Wojciech WIĘCŁAWEK, PhD
Piotr ZARYCHTA, PhD

PhD Students

Monika BUGDOL, MSc
Michał JEŻEWSKI, MSc
Jan JUSZCZYK, MSc
Joanna CZAJKOWSKA, MSc
Marcin RUDZKI, MSc
Przemysław SZABELAK, MSc

Research fields

- Biocybernetics and biomedical engineering - processing of information in medicine
  - Processing of biomedical signals
  - Image processing and analysis
  - Fuzzy sets and systems, neuro-fuzzy systems
  - Pattern recognition
  - Cybernetics
  - Computer assisted medical diagnosis
  - Image guided surgery
  - Hospital information system
  - Picture archiving and communications systems
  - Medical information systems integration
  - Expert systems in medicine
  - Time-frequency analysis of biomedical signals

    - Multirate signal processing
    - Evolutionary computations
    - Artificial neural networks
    - Data mining
    - Artificial intelligence

- Design, construction and testing of electronic medical apparatus
    - Design and construction of amplifiers for biological signals and data acquisition systems co-operating with computers
    - Testing of electromedical apparatus
    - Design of electronic devices for data acquisition

Courses

- Electromedical Metrology
- X-ray and Nuclear Imaging
- Medical Information Systems
- Cybernetics
- Electromedical Equipment
- Pattern Recognition
- Principles of Knowledge Engineering
- Diagnostic Imaging Systems
- Biocybernetics
- Computers in Medicine
- Diagnostic Cardiological Systems
- Computer Aided Medical Diagnosis
- Materials Science and Principles of Construction of Electronic Equipment
- Probability Theory and Mathematical Statistics
- Numerical Methods
- Biomedical Information Processing

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

Head of Division: Prof. Ewaryst TKACZ, PhD, DSc

Research staff

Prof. Ewaryst TKACZ, PhD, DSc

Prof. Sławomir KOŃCZAK, PhD, DSc
Prof. Jacek SZUBER, PhD, DSc
Asst. Prof. Zbigniew PRUSZOWSKI, PhD
Wojciech FILIPOWSKI, PhD
Weronika IZYDORCZYK, PhD
Dariusz KOMOROWSKI, PhD
Paweł KOSTKA, PhD
Piotr KOWALIK, PhD
Monika KWOKA, PhD
Jerzy ULJANOW, PhD
Krzysztof WACZYŃSKI, PhD
Edyta WRÓBEL, PhD

PhD Students

Artur GINTROWSKI, MSc

Research fields

- Biotechnology and bioinformatics
  - Analysis of gene expressions
  - Computer assisted medical diagnosis
  - Time-frequency analysis of biomedical signals
  - Multirate signal processing
  - Evolutionary computations
- Design of electronic devices for data acquisition
- Application of organosilicon compounds to the production of doped glasses for semiconductor technology
- Special hybrid circuits made in thick (thin) film technology
  - Hermetic sealing of hybrid circuits based on epoxy plastics
  - Manufacture and stability testing of resistance ladders based on pastes of Polish production
  - Vapour deposition of metallic layers applied to hybrid circuits
- Chemical compounds for thick- and thin-film sensors
- Solar cells and photovoltaic systems
- Studies on optimization of cleaning and passivation technology of GaAs and InP surfaces in aspects for application in microelectronics

- Studies on optimization of technology of SnO2 nanolayers and CuPc nanolayers in aspects for application in solar batttery and gas sensors

Courses

- Materials Science and Principles of Construction of Electronic Equipment
- Electromedical Metrology
- Bionics
- Computers in Medicine
- Biotechnology in Medicine
- Computer Assisted Diagnostics in Medical Care
- Artificial Organs
- Microelectronics
- Physics of Microfabrication
- Electronic Devices, Semiconductor Structures and Circuits
- Sensors
- Principles of Electron Technology
- Semiconductor Devices
- Special Semiconductor Devices
- Thin-Film Technology
- Thick-Film Technology
- Design of Thick/Thin-Film Circuits
- Hybrid Circuit Technology
- Hermetic Sealing
- Solid-State Physics
- Physics
- Physics in Medicine

STATUTORY ACTIVITES OF THE INSTITUTE OF ELECTRONICS

PhD DEGREES CONFERRED ON STAFF MEMBERS AND PhD STUDENTS OF THE INSTITUTE OF ELECTRONICS

1. **Wojciech Filipowski**, The development and validation of the model to aid the process of diffusion doped design of the photovoltaic cell emitter layer, PhD advisor: Prof. Sławomir Kończak, 24 February 2009
2. **Wojciech Sułek**, LDPC codes effectively decodable with programmable logic devices, PhD advisor: Prof. Dariusz Kania, 24 February 2009
3. **Barbara Mika**, Electrogastrographic (EGG) signals analysis by modern algebraic methods, PhD advisor: Prof. Ewaryst Tkacz, 21 April 2009
4. **Łukasz Ćmielowski**, Comparative analysis of methods examining DNA microarray gene expression data, PhD advisor: Prof. Ewaryst Tkacz, 22 September 2009
5. **Piotr Jantos**, A Diagnosis of Global Parametric Faults in Analogue Integrated Circuits With the Use of Artificial Intelligence Methods, PhD advisor: Prof. Jerzy Rutkowski, 5 December 2009
6. **Łukasz Chruszczyk**, Fault diagnosis of analog electronic circuits using specialised aperiodic excitations, PhD advisor: Prof. Jerzy Rutkowski, 15 December 2009

RESEARCH GRANTS

Research activities of the Institute of Electronics are mainly financed by the Ministry of Science and Higher Education within the frames of a general research programme:

- ***Development of new research areas in electronics, telecommunication and signal processing***

Apart from this, each division of the Institute carries out its own research in the following general areas, which are further subdivided into individual research projects:

Division of Electronics Fundamentals and Radio Engineering:

- *Electronic components, circuits and systems - development of measurement methods, analysis and synthesis*

Division of Digital and Microprocessor Systems:

- *Multiprocessor systems, application specific integrated circuits programmable logic devices and systems - analysis, design and testing*

Division of Circuit and Signal Theory:

- *Computer-aided methods of analysis, synthesis and testing of electronic systems and their selected applications*

Division of Telecommunication:

- *Development of methods and applications of digital channel commutation and transmission of digital signals, theoretical and experimental methods of examination of bodies radiating and dissipating electromagnetic waves*

Division of Biomedical Electronics:

- *Acquisition and processing of biomedical information*

Division of Microelectronics and Biotechnology:

- *Application methods of microelectronic technologies and biotechnologies*

In total, forty five individual research projects were completed in 2009.

GRANTS AWARDED BY THE COMMISSION OF EUROPEAN COMMUNITIES

VI Framework Programme of European Union

Network of Excellence - General Olfaction and Sensing Projects on a European Level – GOSPEL Contract EC: IST 507610 Period: 2004-2008 (completed 09.2009) Coordination: Dr. Udo WEIMAR, University Tubingen, Germany. Role in project: research partner and Member of Steering Committee of Network, (Prof. J. Szuber)

VII Framework Programme of European Union

Structural Project – Operational Programme of Innovative Economy

Innovation Technology of Multifunctional Materials and Structures for Nanoelectronics, Photonics, Spintronics and Sensoric Techniques (InTechFun), Period: 2009-2013, Role in project: Prof. J. Szuber - Head of the group PSl-2

The project deals with the development of a new innovative technology of multifunctional materials and structures for nanoelectronics, photonics, spintronics and sensoric techniques. It has a form of a national network with the contribution of 6 Polish partners from academia and industry. The Institute of Electronics is responsible for 5 Workpackages dealing with technology and characterization of novel materials, structures and prototypes. Moreover, one Workpackage is devoted to the modernization of experimental systems for nanotechnological application. The project started on May 2009 and within this year the general organizational scheme for research and development was developed together with the implementation of experimental systems for future studies.

INDIVIDUAL RESEARCH GRANTS AWARDED BY THE MINISTRY OF SCIENCE AND HIGHER EDUCATION TO STAFF MEMBERS OF THE INSTITUTE

1. **Prof. E. Tkacz**, Elaboration of the New Methodology for Electrogastrographic Signals Examination Concerning Identification of Human Multi-channel EGG Characteristic Parameters Repeatability
2. **Prof. E. Piętka**, Computer added evaluation of the demyelination process in multiple sclerosis
3. **Prof. E. Piętka**, Photodynamic image archiving, analysis and communication system in cancer diseases
4. **Prof. A. Karwowski**, Fast hybrid methods of computational electromagnetics, (duration: 18.05.2008 - 18.05.2011)
5. **Prof. A. Karwowski**, Antennas for modern wireless systems for information society technologies - new structures, models, and methods of analysis and design (2009-2011)
6. **Prof. J. Szuber,** Special Research Programme, Network of Excellence: Sensoric Projects on a European Level Period: 2004-2008 (completed 09.2009)
7. **Prof. J. Szuber**, Studies of local morphology and stoichiometry of tin dioxide SnO_2 thin films prepared by RGTO technology in aspect for sensoric application, (2007-2009)
8. **W. Sułek (MSc)**, (PhD grant, advisor: Prof. D.Kania), LDPC codes effectively decoded with programmable logic devices

INTERNATIONAL CO-OPERATION

1. Technical University of Ostrava, Department of Measurements and Control, Czech Republic (Prof. E. Hrynkiewicz)
2. University of Southern California (Prof. E. Piętka)
3. SECTRA – Sweden (Prof. E. Piętka)
4. Chemnitz University of Technology, Germany (Prof. J. Szuber)
5. University of Tübingen, Germany, (Prof. J. Szuber)
6. Ecole Centrale de Lyon, Ecully, France, (Prof. J. Szuber)
7. University Clermont-Ferrand, France, (Prof. J. Szuber)

8. University of L'Aquila, Coppito, Italy, (Prof. J. Szuber)
9. Graz University of Technology, Austria, (Prof. J. Szuber)
10. Hokkaido University, Sapporo, Japan, (Prof. J. Szuber)
11. Kyushu University, Fukuoka, Japan, (Prof. J. Szuber)
12. Technical University of Prague, Institute of Bioengineering, Czech Republic (Prof. E. Tkacz)
13. Technical University of Stuttgart, Institute of Bioengineering, Germany (Prof. E. Tkacz)
14. California University, Department of Electrical Engineering and Computer Science, Berkeley, USA (Dr. A. Pułka)
15. Université Henri Poincaré, Nancy, France (Dr. N. Henzel)

SCIENTIFIC CONFERENCES ORGANISED AND CO-ORGANISED BY THE INSTITUTE OF ELECTRONICS

1. VI International Workshop on Semiconductor Surface Passivation, Zakopane, 13-18 September 2009, General Chairman: Prof. J.Szuber, Guest Editor of Proceedings in Applied Surface Science (Elsevier)
2. International Conference IMAPS – IEEE CPMT Poland, Gliwice – Pszczyna, 21-24 September 2009, Chairman: Dr. K. Waczyński
3. IFAC Workshop on Programmable Devices and Systems (PDeS 2009), Ostrava, Czech Republic, 10–12 February 2009, (co-organization - Prof. E. Hrynkiewicz)

STAFF MEMBERS PARTICIPATING IN SCIENTIFIC AND ORGANISING COMMITTEES OF CONFERENCES AND SYMPOSIA

International

1. **Dr T. Garbolino**, Steering Committee and Program Committee, 12th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2009, 15-17 April 2009, Liberec, Czech Republic
2. **Dr K. Gucwa**, Program Commitee, 12th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2009, 15-17 April 2009, Liberec, Czech Republic
3. **Prof. A. Hlawiczka**, Steering Committee Honorary Member and Program Committee, 12th IEEE Workshop on Design and Diagnostics

of Electronic Circuits and Systems, DDECS 2009, 15-17 April 2009, Liberec, Czech Republic

4. **Prof. E. Hrynkiewicz**, Program Committee, IFAC Workshop on Programmable Devices and Systems (PDeS'09), Ostrava, Czech Republic, 10–12 February 2009
5. **Prof. E. Hrynkiewicz**, Steering Committee and Program Committee, 12th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2009, 15-17 April 2009, Liberec, Czech Republic
6. **Prof. E. Hrynkiewicz**, Program Committee, International Conference IMAPS – IEEE CPMT Poland, Gliwice-Pszczyna, 21-24 September 2009
7. **Prof. A. Karwowski**, International Steering Committee, EMC Europe 2009, Athens, Greece, 11-12 June 2009
8. **Dr. A. Pawlak**, Steering Committee and Program Committee, 12th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems, DDECS 2009, 15-17 April 2009, Liberec, Czech Republic
9. **Dr. A. Pawlak**, Program Committee member**,** 10th IFIP Working Conference on Virtual Enterprises, PRO-VE09, 7-9 October 2009, Thessaloniki, Greece
10. **Dr. A. Pawlak**, Program Committee member, the Second International Conference on Advances in Circuits, Electronics and Microelectronics, CENICS09, 11-16 October 2009, Sliema, Malta
11. **Dr. A. Pawlak**, Program Committee member**,** International Conference on Intelligent Interactive Assistance and Mobile Multimedia Computing, IMC2009, 11-13 November 2009, Rostock, Germany
12. **Dr. A. Pawlak**, Program Committee member, 12th EUROMICRO Conference on Digital System Design, DSD09, 27-29 August 2009, Patras, Greece
13. **Prof. J. Szuber**, General Chairman, 6th International Workshop on Semiconductor Surface Passivation, Zakopane, Poland, 13-18 September 2009
14. **Prof. E. Tkacz,** Program Committee, International Conference IMAPS – IEEE CPMT Poland, Gliwice-Pszczyna, 21-24 September 2009

National

1. **Prof. Z. Filus,** 8th National Electronics Conference, 7-10 June 2009, Darłówko Wschodnie
2. **Prof. E. Hrynkiewicz**, 8th National Electronics Conference, 7-10 June 2009, Darłówko Wschodnie
3. **Prof. E. Hrynkiewicz**, 12th National Conference Reprogrammable Digital Circuits, RUC 2009, 28-29 May 2009, Szczecin
4. **Prof. E. Hrynkiewicz**, Scientific Conference „Informatics – Art. Or Craft?" and Training Workshop of the Institute of Computer Science and Electronics of the Zielona Góra University, 3-5 June 2009
5. **Dr. J. Izydorczyk,** IEEE Poland Section Chapter Chair, coordinator of the IEEE technical cosponsoring, Conference Computer Networks, 16-20 June 2008, Zakopane
6. **Prof. D. Kania**, 12th National Conference Reprogrammable Digital Circuits RUC 2009, 28-29 May 2009, Szczecin
7. **Prof. D. Kania**, Scientific Conference „Informatics – Art. Or Craft?" and Training Workshop of the Institute of Computer Science and Electronics of the Zielona Góra University, 3-5 June 2009
8. **Prof. L. Lasek**, 8th National Electronics Conference, 7-10 June 2009, Darłówko Wschodnie
9. **Prof. E. Piętka**, Conference Databases – Applications and Systems, 26-29 May 2009, Ustroń
10. **Prof. J. Rutkowski,** 8th National Electronics Conference, 7-10 June 2009, Darłówko Wschodnie
11. **Prof. J. Rutkowski**, Conference Computer Networks, 16-20 June 2009, Zakopane
12. **Prof. J. Rutkowski**, Conference Databases – Applications and Systems, 26-29 May 2009, Ustroń

REVIEWERS

1. **Dr. R. Czabański**, Fuzzy Sets and Systems; IET Control Theory & Applications; Hindawi Publishing Corporation; Applied Mathematics and Computer Science
2. **Dr. T. Garbolino,** reviewer of EU project proposals
3. **Dr T. Golonek**, IEEE Transactions on Circuits and Systems II

4. **Dr. D. Grzechca**, International Journal of Circuit Theory and Application; Metrology And Measurement Systems
5. **Prof. A. Hławiczka**, grant proposals for the Czech Grant Agency (since 2000)
6. **Prof. E. Hrynkiewicz,** grant proposals for the Czech Grant Agency (since 2000); International Journal on Applied Mathematics and Computer Science; IFAC PDeS, IEEE – ICSES, IEEE DDECS Symposium, Conference on Reprogrammable Digital Devices
7. **Dr. J. Izydorczyk,** IEEE Transactions on Magnetics; IEEE Transactions on Circuits and Systems I, Physica B - Condensed Matter, 7th International Conference on Education and Information Systems, Technologies and Applications EISTA 2009, International Symposium on Engineering Education and Educational Technologies EEET 2009, The First International Conference on "Networked Digital Technologies"
8. **Prof. D. Kania,** International Journal on Applied Mathematics and Computer Science, Bulletin of the Polish Academy of Science
9. **Prof. A. Karwowski,** IET Proceedings Microwaves, Antennas & Propagation (London); Electronic Letters; IEEE Transactions on Antennas and Propagation; IEEE Transactions on Microwave Theory and Techniques; International Symposium and Exhibition on Electromagnetic Compatibility (EMC)
10. **Dr. P. Kłosowski**, 7th International Conference on Education and Information Systems, Technologies and Applications EISTA2009, 3rd International Multi-Conference on Society, Cybernetics and Informatics IMSCI2009, 2nd International Symposium on Engineering Education and Educational Technologies EEET 2010, grant proposoals in the Operational Program Innovative Economy 2007-2013 (Ministry of Science and Higher Education)
11. **Dr. D. Komorowski**, 31th Annual International IEEE EMBS Conference
12. **Dr. J. Konopacki,** IEEE Signal Processing Letters; IEEE Transactions on Circuits and Systems - Part II; IEEE Transactions on Signal Processing; IEEE Transactions on Circuits and Systems I, IEEE International Conference on Electronics, Circuits and Systems

13. **Dr. M. Kotas**, IEEE Transactions on Biomedical Engineering; Computer Methods and Programs in Biomedicine; Biomedical Signal Processing and Control

14. **Prof. J. Łęski**, Medical Technology in Medical Science Monitor; IEEE Transactions Neural Networks; International Journal Applied Mathematics and Computer Sciences; IEEE Transactions Systems, Man & Cybernetics; Journal of Applied Computer Science; European Journal of Operational Research, Fuzzy Sets and Systems; Pattern Recognition Letters; IEEE Transactions Biomedical Engineering; IEEE Transactions Fuzzy Systems; Journal of Theoretical and Applied Mechanics; IEEE Transactions Signal Processing; Computational Statistics and Data Analysis; Bulletin of the Polish Academy of Sciences; BioMedical Engineering OnLine

15. **Dr. A. Noga**, Progress In Electromagnetics Research, Journal of Electromagnetic Waves and Applications

16. **Prof. E. Piętka,** CARS – Computer Assisted Radiology and Surgery; EuroPACS (European PACS Society); CORES; IEEE Transactions on Medical Imaging; Computerised Medical Imaging and Graphics; Medical Science Monitor; European Journal of Operational Research; Modelling and Simulation in Engineering VLSI Design; Journal of Applied Mathematics and Computer Science; Journal of Medical Systems; British Medical Journal

17. **Dr. A. Pawlak**, International Conference on Management of Emergent Digital EcoSystems MEDES09, **s**pecial issue of the International Journal on Production Planning & Control **(**about Engagement in Collaborative Networks), PRO-VE08; EU projects and project proposals concerning embedded systems; nanoelectronics, collaborative networks); Internet of Things & Enterprise environments, grant proposoals in the Operational Program Innovative Economy 2007-2013 (Ministry of Science and Higher Education), International Journal of Applied Mathematics and Computer Science

18. **Dr. A. Pułka**, reviewer of EU projects and project proposals; IEEE Transactions on Instrumentation and Measurement; IEEE ICECS (International Conference on Electronics Circuits and Systems)

19. **Prof. J. Rutkowski**, IEEE Transactions on Computer Aided Design (CAD)

20. **Dr. E. Straszecka**, Information Sciences, International Journal Elsevier

21. **Prof. J. Szuber**, Applied Surface Science, Thin Solid Films, Sensors and Actuators B (Elsevier), International Symposium on Olfaction and Electronic Nose, (journal: Sensors and Actuators B), VI International Workshop on Semiconductor Surface Passivation (journal: Applied Surface Science), 4th Symposium on Vacuum based Science and Technology (journal: Vacuum (Elsevier)), XI Seminar PTP – Surface and Thin Films Structures (journal: Optica Applicata), III Conference on Nanotechnology (journal: Acta Physica Polonica B), national project proposals (Ministry of Science and Higher Education)
22. **Prof. E. Tkacz,** grant proposals for the Czech Grant Agency, IEEE Transactions on Biomedical Engineering; Elsevier Signal Processing
23. **Dr. D. Wójcik**, Progress In Electromagnetics Research, Journal of Electromagnetic Waves and Applications

OTHER IMPORTANT AFFILIATIONS

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3. **Prof. A. Hławiczka**, member of the Steering Committee of the European Dependable Computing Conference (EDCC) and the European Workshop (EWDC)
4. **Prof. E. Hrynkiewicz**, member of the Electronics and Telecommunication Committee, Polish Academy of Sciences
5. **Prof. E. Hrynkiewicz**, Chairman of the section Electronics at the Katowice Branch of the Polish Academy of Sciences
6. **Prof. E. Hrynkiewicz**, Section on Signals, Circuits and Systems of the Electronics and Telecommunication Committee, Polish Academy of Sciences
7. **Prof. E. Hrynkiewicz**, Microelectronics Section of the Electronics and Telecommunication Committee, Polish Academy of Sciences
8. **Prof. E. Hrynkiewicz**, member of IFAC Technical Committee TC 4.1 on Components and Technologies for Control

9. **Dr. J. Izydorczyk**, Chairman of Computer Society Chapter, Poland Section IEEE
10. **Dr. J. Izydorczyk**, Senior Member of the Institute of Electrical and Electronics Engineers (IEEE)
11. **Dr. J. Izydorczyk**, Przewodniczący sekcji polskiej towarzystwa komputerowego IEEE (C-016) (kadencja 2008-2009).
12. **Prof. D. Kania**, member of the section Electronics at the Katowice Branch of the Polish Academy of Sciences
13. **Prof. D. Kania**, Section on Signals, Circuits and Systems of the Electronics and Telecommunication Committee, Polish Academy of Sciences
14. **Prof. A. Karwowski**, founder and Chairman of the Polish Chapter of the IEEE Electromagnetic Compatibility Society
15. **Prof. A.Karwowski,** member of the International Steering Committee of EMC Europe -- International Symposia and Workshops on Electromagnetic Compatibility
16. **Prof. A. Karwowski**, Vice-Chairman of the Antennas and Propagation Society, AP/AES/MTT Joint Chapter of the IEEE Poland Section
17. **Prof. A. Karwowski**, member of the 4th Workgroup (WG 4) "Characterization of high frequency electromagnetic fields and SAR produced by specific sources", Technical Committee 106 "Methods for the assessment of electric, magnetic and electromagnetic fields associated with human exposure" of the International Electrotechnical Commission (IEC)
18. **Prof. A. Karwowski,** member of the Project Team (PT) 62209 "Human Exposure to Radio Frequency Fields from Handheld and Body-Mounted Wireless Communication Devices - Human models, Instrumentation, and Procedures", Technical Committee 106, IEC
19. **Prof. A. Karwowski,** member of the Project Team (PT) 62232 "EM fields from base stations for mobile telephone", Technical Committee 106, IEC
20. **Prof. A. Karwowski,** member of the Technical Committee 104 for Electromagnetic Compatibility of the Polish Standardisation Committee

21. **Prof. A. Karwowski**, member of the Electromagnetic Compatibility Section, Electronics and Telecommunication Committee, Polish Academy of Sciences
22. **Prof. A. Karwowski**, member of the Microwave Section, Electronics and Telecommunication Committee, Polish Academy of Sciences
23. **Dr. J. Konopacki,** Secretary of the section Electronics at the Katowice Branch of the Polish Academy of Sciences
24. **Prof. J. Łęski**, member of the division Fuzzy Logic and Neural Networks at the section Automatics and Robotics of the Polish Academy of Sciences, Polish Biomedical Engineering Society
25. **Prof. J. Łęski**, member of the Scientific Committee of the Biomedical Engineering Centre
26. **Prof. J. Łęski**, member of the Scientific Committee of the Institute of Medical Technology and Equipment
27. **Prof. J. Łęski**, member of the section Electronics at the Katowice Branch of the Polish Academy of Sciences
28. **Prof. J. Łęski**, member of the Steering Committee at the Gliwice-Opole Branch of the Polish Society of Theoretical and Applied Electrotechnics
29. **Prof. J. Łęski,** Senior Member IEEE
30. **Dr. A. Pawlak**, member of IFIP (International Federation for Information Processing) W.G. 10.5 "Electronic Systems Description and Design Tools"
31. **Dr. A. Pawlak**, correspondent of EUROMICRO Association, IFIP (International Federation for Information Processing) W.G. 10.5 "Electronic Systems Description and Design Tools"
32. **Dr. A. Pawlak**, member of SOCOLNET **(**Society of Collaborative Networks)
33. **Dr. A. Pawlak**, member of the Steering Committee of the European Workshop on Design and Diagnostics of Electronic Circuits and Systems (DDECS)
34. **Prof. E. Piętka**, IEEE Poland Section - Engineering in Medicine and Biology - chair of the EMS Chapter
35. **Prof. E. Piętka**, member of the Board of European PACS Society (EuroPACS)

36. **Prof. E. Piętka**, member of the Programme Committee of Computer Assisted Radiology and Surgery
37. **Prof. E. Piętka**, member of the Programme Committee of European Congress of Radiology
38. **Prof. E. Piętka,** member of the Section Electronics at the Katowice Branch of the Polish Academy of Sciences
39. **Dr. A. Pułka**, member of Chess (Center for Hybrid and Embedded Software Systems) at the University of California
40. **Prof. J. Rutkowski**, Section on Signals, Circuits and Systems of the Electronics and Telecommunication Committee, Polish Academy of Sciences
41. **Prof. J. Rutkowski**, member of the Electronics and Telecommunication Committee of the Polish Academy of Sciences - Microelectronics Section
42. **Prof. J. Rutkowski**, member of the Accreditation Commission of Technical Universities in Poland - Electronics and Telecommunication Section
43. **Prof. J. Rutkowski**, Steering Committee member of the Electronics and Telecommunication Panel of the Polish Academy of Sciences
44. **Prof. J. Szuber**, member of the Committee of Metrology and Scientific Apparatus – Section of Microsystems and Measuring Sensors, Polish Academy of Science
45. **Prof. J. Szuber**, International Union on Vacuum Science, Technology and Application (IUVSTA), Representative of Polish Vacuum Society
46. **Prof. J. Szuber**, Polish Vacuum Society, Member of General Board – President Elect for the period 2008-2011
47. **Prof. E. Tkacz,** member of the International Advisory Board of the Annual Journal of Medical Informatics and Technology published by the University of Silesia
48. **Prof. E. Tkacz,** member of the Section Electronics at the Katowice Branch of the Polish Academy of Sciences

PATENTS AND PATENT APPLICATIONS

Adam Kristof (PhD), Patent application No. P-387902 of 28 April 2009, "Circuit Structure of Push-Pull Current Output Power Amplifier"

Piotr Kyzioł (MSc), Damian Grzechca (PhD), Prof. Jerzy Rutkowski, Patent application No. P-388434 of 01 July 2009, „Tester for analog electronic circuit diagnosis"

Damian Grzechca (PhD), Patent application No. P-388781 of 11 August 2009, "System for Initial Identification of the Phone Caller"

Grzegorz Wieczorek (PhD), Patent application No. P-390277 of 08 December 2009, "Method and apparatus for metal object detection"

OTHER IMPORTANT INFORMATION

In March 2009 our university hosted Prof. Metin AKAY from Harrington Department of Bioengineering, Arizona State University, invited by the IEEE EMBS Poland Chapter (Prof. J. Rutkowski, Prof. E. Tkacz). On 17 March 2009 he presented a lecture entitled "Neural Engineering in the Global Health Care" at the Institute of Electronics.

In May 2009 two students of Electronics and Telecommunication, Przemysław Flak and Piotr Foltyn, won the first prize in the Digilent Design Contest at the Technical University of Cluj-Napoca, Romania. This competition is sponsored by Digilent and Xilinx.

On 19 May 2009 the Institute of Electronics (Dr. D. Wójcik) and the EMC-Society Chapter IEEE Poland Section have organised the 2nd Open Radioelectronics Workshop „RF Devices and Systems Design for EMC Control".

LIBRARY RESOURCES OF THE INSTITUTE OF ELECTRONICS

Total number of book titles	6402
Number of subscribed national journals	8
Number of subscribed foreign journals	19

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4. **Chmiel M., Hrynkiewicz E.,** An Idea of Event-Driven Program Tasks Execution, The International IFAC Workshop on Programmable Devices and Embedded Systems, PDeS'09, 10-13 February 2009, Roznov pod Radhostem, Czech Republic, pp. 132-137
5. **Chmiel M., Hrynkiewicz E., Milik A**., Fast Operating PLC Based on Event Driven Control Program Task Execution, Electronics and Telecommunication Quarterly 2009, Vol. 55, no 2, pp. 269 – 286
6. **Chmiel M., Mocha J., Kania D., Hrynkiewicz E**., Dynamic partial reconfiguration of CPU-s for Programmable Logic Controllers executing control programs developed in the Ladder Diagram language, 4rd IFAC Workshop On Discrete-Event System Design, DESDes'09, October 6-8, 2009, Gandia Beach, Spain, pp. 59-64
7. **Chruszczyk Ł., Rutkowski J**., Specialised aperiodic excitation and wavelet transform improves analogue fault diagnosis, The 19th European Conference on Circuit Theory and Design (ECCTD), 23 – 27 July 2009, Antalya, Turkey, pp. 655 – 658
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International Interdisciplinary Technical Conference of Young Scientists (InterTech), 20 - 22 May 2009, Poznań, pp. 138 – 142

9. **Czajkowska J., Badura P., Pietka E**., An approach to the pleura-connected and vascularized lung nodules, Int. J. of CARS, Vol. 4, Supp. 1, 2009, pp. 362-363

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13. **Czerwiński R., Kania D**., Synthesis of Finite State Machines for CPLDs, International Journal of Applied Mathematics and Computer Science (AMCS), Vol. 19, No. 4, 2009 **(**ISI MJL**)**

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20. **Dziczkowska M.,** Application of the eddy current method for measurement of geometrial dimension in two-layer structures, Mašinostroenie i Technosfera XXI weka. Sbornik Trudow XV Meždunarodnoj Naučno-techničeskoj Konferencji, Donieck 2009, Vol. 4, pp. 62-65

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29. **Filipowski W., Waczyński K., Wróbel E.,** Drabczyk K., Effective coefficient of phosphorus diffusion in silicon for doping emitter layer of solar cell, XXXIII International Conference of IMAPS-CPMT IEEE Poland, Pszczyna, 21-24 September 2009, pp.126-131

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36. **Fiołka J., Kidoń Z.,** A Method for verification of stabilographic data collection process, Elektronika, No. 10, 2009, pp. 51-54 (reprint from the National Electronics Conference)

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ABSTRACTS OF SELECTED RESEARCH PROJECTS

DIVISION OF ELECTRONICS FUNDAMENTALS AND RADIO ENGINEERING

Prof. A. Karwowski, M. Surma (PhD), D. Wójcik (PhD), *Efficient wide-band rational macromodels of radiating/scattering structures*

Investigation of the broadband performance behaviour of radiating/scattering structures via full-wave numerical simulation in the frequency domain is usually performed by evaluating samples of the desired observable with a uniform frequency step within the band of interest. The overall process may be time consuming and resource demanding. Therefore, the techniques offering reduction of the simulation costs are highly desirable. One of possible approaches aimed at speeding up the electromagnetic simulation consists in reducing the order of a model and constructing a macromodel of the EM system.

Within this research we have examined robust macromodeling approaches for rational approximation of frequency domain responses. In the first approach attention is focused on a simulation technique employing the Neville-type Stoer-Bulirsch (SB) rational interpolation algorithm combined with the adaptive-frequency sampling (AFS) technique. The SB algorithm is a recursive tabular technique aimed at determining the value of the interpolating rational function for a single frequency. The algorithm does not require matrix inversion and can process a relatively large number of supporting points without suffering from ill-conditioning. This inherent feature of the algorithm makes it an exceptionally attractive candidate for constructing rational interpolation of a system response over a broad frequency band.

The second approach to wide-band rational macromodelling is dedicated to efficient transient response analysis of radiating/scattering objects. The frequency-domain response is analyzed initially by the method of moments (MoM) combined with the asymptotic waveform evaluation (AWE) technique. The MoM/AWE approaches the frequency response as a set of rational functions: each function describes the behavior of the observable over certain frequency subrange. However, partitioning of the frequency response does not enable to obtain the transient response analytically by using the inverse Laplace transform. To overcome this limitation, the vector fitting technique is employed. The VF is a robust macromodelling tool that circumvents ill-conditioning problems which usually occur in high order rational approximations. The

technique is a reformulation of Sanathanana-Koerner iterations which uses a partial fraction basis instead of the polynomial basis. The VF leads to approximation of the frequency response by one rational function covering the whole frequency range, ensuring also stability and passivity of the response, which is not taken into account by the MoM/AWE algorithm.

A. Kristof (PhD), *Circuit structures of linear wideband power amplifiers*

The general goal of this research project is defined as detailed analysis of structural solutions found in amplifier circuits and definition of relationships between the applied structural (circuit) solutions and the obtained or possible to obtain properties of the amplifier circuit. Linear wide-band push-pull amplifiers are a special field of interest. In the recent years the research work was related among other things to: general principles of operation of the electrical signal amplifiers and the resulting possibilities of realization of amplifying circuits; the energetic efficiency of amplifiers operated in classes G and H; a method of quick estimation of efficiency for class D amplifiers; methods of minimizing the power losses in class AB amplifiers and the utilization of negative feedback loop for modeling of output impedance in order to improve the frequency power response of the whole amplifier - loudspeaker system.

Some theoretical results of the performed research include derivation of analytical formulas for power losses and energetic efficiency of amplifiers operating either in class G or in class H, a proposal of a simplified method which enables analysis of real power losses in class D amplifiers upon only two coefficients, development of an original method of linearization of power transistors in class B amplifiers and an original amplifier circuit structure which results from this method, analysis of the amplifier output impedance modeling problem in context of achieving optimal cooperation of the amplifier with load, and literature research of the approach and solutions described as „super-class-AB", which enable implementation of push-pull R2R-output (Rail-to-Rail) amplifiers of very high efficiency and of very good dynamic properties.

Among the more significant practical results there are: a circuit structure of a hybrid tube-transistor amplifier; a prototype class D amplifier with sigma-delta processing; a typical solution of push-pull amplifier based on monolithic voltage regulators; and both a circuit structure and a prototype of a wideband power amplifier with current output. In the hybrid tube-transistor amplifier the tubes operate as the main power distributing elements and the transistor subcircuits have a task of linearization and of precise biasing of each power tube. One of the essential advantages of this solution is low sensitivity to a change of tube parameters, and thus low influence of tubes "ageing" on amplifier's parameters. In the push-pull amplifier based on monolithic voltage regulators the latter operate as the main power distributing elements. The circuit structure of a wideband push-pull power amplifier with the current output offers some interesting properties, which allow to leave out the circle of some design and engineering habits. First of all, the output signal in this solution is current rather than voltage. The traditional global

voltage negative feedback loop cannot be used in this solution, because it would have an undesirable influence on the amplifier's output resistance. However, negative feedback is used for linearization of the power transistors, and thus the current output amplifier may show excellent linearity. Another advantage of the current output amplifiers is their high immunity to short circuits and overloads.

Z. Rymarski (PhD), *Single-phase and three-phase voltage source inverters for UPS systems*

The research concerns a general design method of voltage source inverters for UPS systems that minimises the number of sensors and does not need a very powerful microprocessor in the control system (e.g. the control does not need calculating the time consuming relations of Kalman's filter that estimates the unmeasured state variables). The algorithms for a complete design of a single and three-phase VSI have been formulated. The choice of PWM type and its scheme (the sequence of the power switches control), based on a harmonic analysis of the unfiltered waveform of the voltage source inverter output and graphical interpretation of this analysis for two separate frequency ranges in a function of the basic PWM parameters such as the modulation depth ratio and the carrier to fundamental frequencies ratio, has been justified. Simple formulas that enable the calculation of the output filter of the single- or three-phase VSI have been worked out based on the limitations set on the output filtered voltage distortion level and on the minimisation of the reactive power in the output filter components. The ranges of parameters have been found for which it is possible to effectively decrease the output filtered voltage distortions for a nonlinear load. The output power stage, including the output filter, was described by means of difference equations for the different state variables vectors, taking into account the parasitic parameters of the filter and the previously calculated dependencies of the filter parameters on the carrier frequency and the nominal resistance load. The discrete models of the inverter together with the PWM modulator (different for the single and double-edge PWM) have been elaborated, including previous calculations of the filter parameters which enable the direct design of the discrete controller with the parameters depending on the type of PWM. The discrete PID/CDM (coefficient diagram method) controller was implemented in the inner inverter control loop, enabling sufficient robustness of the system for the load change by means of the choice of the proper time constant of the closed loop system. The RPC (repetitive) controller was implemented in the outer control loop, whose design was significantly simplified owing to the flat Bode characteristics of the inverter with the PID/CDM inner loop. The inner PID/CDM loop damps dynamic, aperiodic disturbances, the outer RPC loop is necessary for rejecting the periodic disturbances and minimizing the output voltage static error. The formulated algorithms were initially checked by means of simulations and finally verified by means of the experimental model. They include the choice of the PWM type and scheme, the output filter design, the VSI topology and the difference equations describing a PID/CDM&RPC controller that can be directly implemented in the software of the microprocessor controlling the VSI. These algorithms enable practical design of a

single- or three-phase VSI using the simple formulas and tables with the coefficients of the control functions presented. The VSI design described was compared by means of simulations with the voltage source inverters controlled by means of alternative methods well known from references and the results of simulations were similar.

DIVISION OF DIGITAL AND MICROPROCESSOR SYSTEMS

R. Czerwiński (PhD), Prof. D. Kania, *Synthesis of Finite State Machines for CPLDs*

This work addresses the problem of Finite State Machines (FSMs) synthesis, targeting their implementation in Complex Programmable Logic Devices (CPLDs). The function of each block is limited by the number of implicants it can handle. This feature affects significantly the synthesis process of digital circuits based on PAL-based devices.

The research work concerns two problems: PAL-oriented state assignment and PAL-oriented multi-level optimisation. The two-step method aims at the area minimization.

One of the most important stages of FSMs' design flow is the state assignment. The aim of the proposed state assignment method is to minimize the number of the PAL-based macrocells by fitting the FSM to the structure of the CPLD. Elements of two-level minimization are included in the state assignment process. The developed primary and secondary merging conditions enable to include elements of two-level minimization in the process of state assignment.

The proposed PAL-based multi-level optimisation allows a considerable reduction of the number of required logic blocks. The main idea of the method is based on a search for shared mutli-output implicants based on the graph of outputs. To increase the effectiveness of this search, the exchange of codes procedure is carried out after the state assignment.

Adjustments of state assignment to logical resources characteristic for a PAL-based logic block allow significant improvement of synthesis effectiveness in relation to other approaches. Moreover, it is worth noting the fact that the achieved FSMs are self-correcting. The reason for this is usage of the coding words with all inactive output levels. The proposed method is an alternative to the FSMs classical technology mapping based on classical coding (binary, one-hot, Gray) with elements of two-level minimization of individual single-output functions and others academic methods like YEDI, NOVA, etc. The results of experiments presented in the authors' publications prove that the proposed synthesis method is especially attractive for CPLD structures consisting of small PAL-based logic blocks.

Prof. E. Hrynkiewicz, Prof. D. Kania, M. Chmiel (PhD), A. Milik (PhD), J. Mocha (MSc*), Improving construction and operation speed of a PLC*

In this research project, we first elaborated a method for hierarchical description of control algorithms with their subdivision into tasks that are executed sequentially and those that run concurrently. The proposed method is based entirely on components available in the Ladder Diagram (LAD) language and can be considered as an alternative to the Sequential Function Chart (SFC) diagrams. In addition, an architecture for a reconfigurable logic controller was proposed, which is capable of executing the control program combining hardware and software tasks. For that purpose the mechanism of dynamic partial reconfiguration of programmable gate arrays (FPGA-s) is used. This makes it possible to download to the programmable structure only those tasks which are currently required by the running control algorithm. Such a hardware implementation of the controller enables effective execution of concurrent control tasks by parallel operation of the control-calculation units. Finally, the proposed controller architecture allows using a programmable device with a reduced size, and this makes the solution more cost-effective.

Next we introduced a modified idea of program execution in PLCs. Instead of the serial cyclic execution of the control program an event-driven execution is proposed. The suggested approach to the program execution allows selective execution of program parts or tasks provided that the calculation condition for this part has changed since the last time. This way only these blocks from the entire program are executed whose variables have changed since the last calculation. The proposed method can be implemented as software modification or as hardware accelerated solution. The most important part of the idea is the computation of the task or subprogram triggering condition. In order to determine program blocks that require recalculation in the current program scan execution specific hardware support is planned to be researched. The memory content change detection unit allows to determine changes in the memory content since the last program block execution.

Prof. A. Hławiczka, T. Garbolino (PhD), K. Gucwa (PhD), T. Rudnicki (PhD), *Effective BIST structures for Crosstalk Faults in Interconnects*

The use of deep submicron (DSM) technologies in manufacturing of today's integrated circuits leads to an increase of parasitic coupling capacitances between geometrically adjacent wires. Consequently, this is a source of severe crosstalk noise that may substantially depreciate functionality of the system. Interconnects need to be tested at-speed what requires using a specific BIST structure.

A classical LFSR TPG is infeasible for testing crosstalks because in order to detect faults of this type, specific two-test patterns have to be applied. Such two-test patterns cannot be generated with a typical LFSR. The research group proposed and investigated two BIST structures for testing crosstalk faults in an Interconnect Network Under Test

(INUT) containing n-lines. The first structure uses the Test Pattern Generator (TPG) in the form of a specific LFSR and a separate Output Response Analyser (ORA), while the second uses the Ring LFSR (R-LFSR) being both the TPG and ORA. In both methods the TPG is composed of 2n flip-flops. Every second output of the LFSR is connected to the INUT. Simulation-based experiments were carried out to verify effectiveness of vector sequences produced by the proposed TPG in detection of crosstalk faults provoked at a victim net by simultaneous occurrence of rising (falling) edges 01(10) at k aggressor lines. Crosstalk faults causing occurrence of a positive (negative) glitch at a victim line having a constant value 00(11) as well as the ones that make the edge delayed with an opposite direction 10(01) at a victim line were taken into consideration. Experimental results demonstrated that for $n \in \{8,12,16,20,24,28,32\}$ and $k << n$ all above-mentioned crosstalk faults can be detected by a test sequence of acceptable length.

DIVISION OF CIRCUIT AND SIGNAL THEORY

J. Konopacki (PhD), *Design of infinite impulse response digital filters - selected problems*

The work deals with design of infinite impulse response (IIR) digital filters. Generally, we can distinguish two main techniques of IIR filters design. The first is based on the transformation procedures of an analog prototype filter into a digital filter. The second uses numerical methods to design a digital filter in a direct way. The frequency transformations are the essential element of the first design technique. They allow to obtain the transfer function of the desired filter type from the lowpass transfer function. Such transformations can be applied to the analog prototype filter as well as to its digital counterpart, while designing IIR digital filters. In the field of digital filters design, besides the methodologies based on the standard frequency transformations (that convert a lowpass filter into a highpass, bandpass or bandstop filter), the high-order transformations and frequency transformations for complex filters could be performed. The latter transformations allow to obtain multiband filters and filters described by a transfer function with complex-valued coefficients. A frequency transformation can be performed by matrix operation, i.e. the transfer function coefficients of the desired filter are obtained as a result of multiplication of the transformation matrix and the vector composed of the lowpass filter coefficients. In the work the original algorithms of the calculation of the transformation matrices for analog and digital filters of any order are described. The application of these algorithms to IIR filters design is also described.

The direct methods of IIR filters design are considered in the next part of the dissertation. These methods are based on the optimal approximation of the prescribed magnitude and phase responses. Usually in such approaches, the complex-valued error function is defined and then it is minimized with respect to the desired transfer function coefficients. The optimization process must be performed in a way that guarantees

obtaining a stable filter. Some of the modern algorithms of IIR filters design, based on a weighted squares method, are described in this work. They allow to obtain the least squares or the min-max approximation of the desired magnitude response and approximately a linear phase in the passband. The filter order and the group delay of the desired frequency response should be determined to facilitate the process of the design of IIR filters. The right value of the group delay provides a stable filter, when an unconstrained optimization is used for the filter design. It should be noted that a problem of the filter order and the group delay evaluation is not solved yet for direct IIR filter design methods. The formulas of the calculatation of the filter order and the group delay of the desired frequency response for selected filter design methods are also introduced in this work.

A practical example of a filter implementation in a radio signal processing system is also presented. The radio-receiver front end with the direct-conversion is described. It is especially useful for wideband signals, such as those of the Wi-Fi WLAN standard operating in the 2.4 GHz band. The receiver consists of three essential elements: the RF-sampling mixer (which adopts a sample-hold circuit), the lowpass filter and the decimator. The filter is necessary to suppress signal aliasing that appears after the decimation process. Due to the high frequency operation an SC filter has been used, but its relevant prototype was a recursive digital cascade integrator comb (CIC) filter. The proposed front end provides flexibility of the receiver needed for a software-defined radio (SDR) architecture. The SDR can be programmed to comply with any radio standard.

A. Pułka (PhD), A. Milik (PhD); *Heterogeneous commonsense reasoning system based on fuzzy default logic – a mathematical model and implementation in programmable logic*

The work is the continuation of research conducted in the previous years and concerns techniques of reasoning that are able to handle cases with incomplete and vague information. A new original approach to modelling of commonsense reasoning has been proposed. This new mechanism called FDL (Fuzzy Default Logic) combines elements of logic programming based on backtracking, CWA (Closed Word Assumption), NaF (Negation as Failure) and CDL (Cumulative Default Logic) with imprecise reasoning based on FL (Fuzzy Logic) extended by new GTU (Generalized Theory of Uncertainty) proposed by professor Zadeh. Fuzzy Default Logic has been developed formally and implemented in the PROLOG language.

A detailed mathematical model of FDL has been defined and proved: The main elements of the theory: FH (Fuzzy Hypothesis), FDR (Fuzzy Default Rule), CR (Credible Set), HR (Hypotheses Reduction) have been defined. Methods for representation of negation, basis extension and revision beliefs have been presented on examples. The FDL mechanism has been expanded by a new technique for hypotheses assessment and selection of the final conclusion. A detailed discussion concerning FDL-based models stability has been presented. The results of theoretical research

become a basis for the prototype hardware implementation of the FDL in FPGA structures. The work on the HDL model has been initialised and it will be continued in the next year.

The results of this research have been published in two books' chapters (publishers Springer–Verlag and In-Tech), and on the international conference Human Systems Interactions HSI'09 in Catania, Italy.

Prof. J. Rutkowski, D. Grzechca (PhD), T. Golonek (PhD), Ł. Chruszczyk (PhD), P. Jantos (PhD), P. Kyzioł (MSc), *Design and verification of diagnostic methods for analog electronic circuits*

Current research has been focused on creation and verification of diagnostic methods for analog electronic circuits. The research team has experience in the field of heuristic, artificial intelligence and soft computing methods, and this knowledge has been utilized for construction of novel diagnosic methods. The research project has been divided into a few tasks where the following methods have been developed:

1. Fault driven test method in the time domain which is based on primary features (e.g. minima) of the circuit response. The method belongs to dictionary techniques where circuit responses are compared with patterns. Next, the secondary (complex) features are calculated (e.g. response derivative). Evolutionary algorithms, differential evolution and gene expression programming are used for dictionary construction based on all primary and secondary features.

2. Frequency reduction method in the AC domain. The method has two steps, where the Particle Swarm Optimization (PSO) algorithm is applied for finding all ambiguity regions and then a deterministic algorithm minimizes a number of ambiguity states.

3. System for identification of a linear circuit transfer function with the use of evolutionary method. The optimization process uses differential evolution with the mutation type DE2 which allows to put appropriate selection pressure within the best genotype region. The final result is composed of zeros and poles for transmittance which allows to verify the actual circuit specification (the method belongs to Specification Driven Test).

4. Principal Component Analysis (PCA) has been applied and verified under the "multitone" optimization problem. The PCA algorithm significantly reduces the number of sinusoidal excitations and puts signals in the ascending order e.g. for an exemplary circuit only 3 frequencies are required to obtain the highest diagnosability.

5. Summary research on finding an optimal piece-wise linear input signal for analog circuit diagnosis. The main aim of the task was to enhance diagnosis with the wavelet transform which is performed on the input current, power supply currents, and the output voltage.

DIVISION OF TELECOMMUNICATION

A. Dustor (PhD), *Spoken language and speaker recognition*

The task of spoken language recognition is to determine the language spoken in an utterance. Since multilingual applications are becoming increasingly popular due to globalization, spoken language recognition has become an essential technology in areas such as multilingual conversational systems, spoken language translation, multilingual speech recognition. Most of the systems rely on two types of features: the acoustic features and the phonotactic features. The acoustic features reflect low-level spectral characteristics, while the phonotactic features represent the phonological constraints that govern a spoken language. Both features have been shown to be effective in a spoken language recognition. In order to obtain good performance, some problems must be overcome. The most important are: high variability of speech signal which is a result of the fact that voice is behavioural biometrics, the limited length of the utterance and a low quality of speech signal. The influence of these factors should be minimized.

Since spoken language recognition (SLR) is based on similarity calculation between the test utterance and the reference model of the language, it is obvious that the problem of a good model construction is crucial. There are many methods applied to SLR to obtain language models. One of the most simple is the vector quantization VQ method. Language is represented as a set of multidimensional code vectors obtained using k-means or the LBG procedure. This set is known as a codebook. During recognition for each vector extracted from a speech segment the nearest neighbor from the codebook is found. The overall normalized distance is used to make a decision about the recognized language. Significantly better results can be obtained if the minimum likelihood approach is applied like in Gaussian mixture models. GMM's possess ability to capture all of the underlying fluctuations and variations of the speaker's voice and as a result they can model some characteristic properties of the spoken language. In this case language is represented in a recognition system as a linear combination of M multidimensional Gaussian probability distributions.

In order to test GMM based spoken language recognition, Matlab application was written. The results obtained for 15 tested languages have shown very promising results.

P. Kłosowski (PhD), *Distance Education at the Silesian University of Technology*

The Distance Learning Platform used by the Silesian University of Technology is based on the modular object-oriented dynamic learning environment. It represents the LMS (Learning Management Systems) technology, a software package designed to help educators create quality online courses. Currently, over 520 online courses are available, created for students of twelve University's faculties. The total number of users exceeds 12,000. The Distance Learning Platform works as a typically

asynchronous e-learning service, but more synchronous e-learning services will be added in the future. The Distance Learning Platform used by the Silesian University of Technology is continually developed. New interesting features are added as new modules to the source code. These new modules implement the up-to-date echnology that appears in web-based e-learning and Internet services.

The Distance Learning Platform has a great potential to create successful e-learning experiences by providing a plethora of excellent tools that can be used to enhance conventional classroom instruction, in hybrid courses, or any distance learning arrangements It significantly contributes to increasing the efficiency of students' education at the Silesian University of Technology.

W. Sułek (PhD), *Architecture Aware Low-Density Parity-Check Codes*

The work is in the domain of error correcting coding methods, which are one of the main research areas in the Division of Telecommunication. Low-density parity-check (LDPC) codes, after their "re-discovery" in the late 1990s, have attracted great research attention due to their excellent error-correcting performance and highly parallel iterative decoding scheme. An LDPC code is defined by its sparse parity check matrix or a corresponding bipartite (Tanner) graph. A lot of works concerning parity check matrix construction for "good" LDPC codes has been published (e.g. PEG algorithm). However, in order to apply flexible and efficient partially parallel decoder architectures, the parity check matrix has to be blockwise partitioned. The class of such structured codes is known as Architecture-Aware LDPC (AA-LDPC).

In order to obtain LDPC codes efficiently decodable with "good" error correcting capabilities, the code graph construction algorithm has been developed. The algorithm consists of two main steps: seed graph construction (where the known PEG method was adopted) and seed graph expansion. In the latter step, an original algorithm has been proposed that can be used for regular and irregular codes of any length and rate. The algorithm aims to reduce the number of low-length cycles with low external connectivity in the Tanner graph. In consequence, it statistically reduces the number of small Stopping Sets and Trapping Sets in the graph, which are harmful to code performance, especially in the low BER (Bit Error Rate) region. A number of AA-LDPC codes has been constructed making use of the proposed algorithm. Performance of the constructed codes in most cases is similar or even a little better than the performance of the respective, known to be "good", LDPC codes that were taken from the classic MacKay's database. However, the main drawback of MacKay's codes is that they are not Architecture Aware.

A configurable LDPC decoder has also been implemented in the form of synthesizable VHDL description. The decoder is capable of decoding any code that has the parity check matrix in the Architecture-Aware form. It is based on the TDMP algorithm and computations make use of the Min-Sum algorithm with correction and the double recursion scheme. The primary target hardware platform is FPGA and Xilinx VirtexII devices were used for decoder verification. The decoder is used for experiments, as it

allows fast simulation of the LDPC coding systems and thus - calculation of the error performance in the low BER region.

DIVISION OF BIOMEDICAL ELECTRONICS

Prof. J. Łęski, *Iteratively reweighted least squares classifier and its kernel version*

The work introduces a new classifier design method based on regularized iteratively reweighted least squares criterion function. The proposed method uses various approximations of the misclassification error, including: linear, sigmoidal, Huber and logarithmic. Using the representer theorem a kernel version of classifier design method is introduced. The conjugate gradient algorithm is used to minimize the proposed criterion function. Furthermore, L1-regularized kernel version of the classifier is introduced. In this case, the gradient projection is used to optimize the criterion function. Finally, an extensive experimental analysis on 14 benchmark datasets is given to demonstrate the validity of the introduced methods.

It is shown that various approximations of the misclassification error can be written as an iteratively reweighted least squares (IRLS) criterion function. The IRLS procedure can be used for a better than squared approximation of the misclassification error as well as it may be used for relaxation of a “force" to the separating hyperplane created by properly classified data. An extensive experimental analysis showing that the proposed classifier design methods are a good alternative, in terms of both generalization performance and computational cost, to the-state-of-the-art algorithm such as the Lagrangian support vector machine. For linear classification the best performance is observed on the ALOG approximation of the misclassification error. For the kernel version of classifier the ALOG and ALIN approximations are the best for the classifier with and without bias, respectively.

E. Straszecka (PhD), *Computer assistance of medical diagnosis*

Computer assistance of medical diagnosis is required nowadays to cope with multiple test results and evaluate their importance for the diagnosis. Therefore, it is important to develop methods which ensure an accurate representation of expert’s knowledge, use training data and create diagnostic rules that are accepted by the majority of medical centres. To this end, uncertainty and imprecision of medical heuristics should be simultaneously evaluated. It is possible when probability-based and fuzzy methods are joined. Research work performed in the Division of Biomedical Electronics shows that good results are obtained in such a diagnosis support when the Dempster-Shafer theory (DST) is combined with the fuzzy set theory (FST). DST is used to evaluate the significance of a diagnostic rule, either heuristic or data-driven, by means of the basic probability assignment. A diagnostic inference is also performed with DST. FST is convenient for interpretation of linguistic values. This is inevitable to use fuzzy databases, which seem to be introduced in the near future. The basic probability

assignment in DST and the sets in FST can be determined for a selected population by means of training data. At the same time, formulation of the rules is permanent. Thus, rules keep their semantic meaning, while linguistic values that are used in them, as well as their weight in the diagnosis, are tuned to the population. In this way, knowledge transfer among diagnostic centres is easy. Such a diagnosis support can be an alternative to expert systems, which turned out to be inconvenient for medical practice. An expert still plays an important role in preparing the rules. The assignment found from data can be combined with the assignment determined by the expert, which improves robustness of the method. The combination of assignments is also useful for generalization of diagnostic knowledge. The assignment that is established for typical cases can be joined with the assignment set up for rare and specific cases. In this way, common symptoms do not impose diagnosis.

Results of testing the suggested method on benchmark databases indicate that it is more effective than reference procedures. Simultaneously, it is intuitively clear for physicians and easy to compute. Therefore, it can be of significant value for practical problems of diagnosis support.

J. Ihnatowicz (PhD), *Quantitative image analysis in large-scale manufacturing industry*

There are a few problems that have to be solved if any of the measuring procedures has to be applied as a daily-routine scenario. These are the considerably limited time of analysis (max. 3-5 minutes from the start to the final report), the sufficient accuracy of measurements which has to be easily verified during the audits, the user-friendly interface even for the untrained staff, the large volume of input data which may vary from several megabytes up to tens of gigabytes (if the mosaic images are analyzed).

Most of measurement procedures apply to the material analysis based on microscopic images in accordance with current international standards, i.e. the analysis of purity of steels (NMI) , the determination of graphite particles in cast iron, the porosity analysis, the layer thickness measurements, the multiphase analysis, the particle analysis (for the cleanliness validation) and the grain size analysis with automatic reconstruction of the grain boundaries. The separate category of the problems is the high-accuracy microscopy scanning of a large area sample (mosaic images).

For the last few years some of the above listed procedures were successfully applied to the daily-routine work in the selected industry laboratories in Poland. In 2009 we concentrated on the automatic porosity analysis in accordance with the VDG P201 standard for the automotive industry. The laboratory stand configuration consists of a modern stereomicroscope AxioObserver, 5-megapixel digital camera AxioCam and computer hardware. The appropriate software for the professional image analysis computer environment KSRun (Zeiss, Germany) was elaborated and implemented. This software includes image acquisition, calibration, preprocessing and automatic analysis of the selected geometric features of pores based on a segmented image. The final printout-ready report includes the porosity codes in accordance with VDG P201.

DIVISION OF MICROELECTRONICS AND BIOTECHNOLOGY

P. Kowalik (PhD); Z. Pruszowski (PhD), *Preparation of the fixed low-resistance metal resistors by multi-stage metallization process*

Chemical metallization is commonly used as a technological method for preparation of fixed metal resistors. For the case of Ni-P layers the divalent nickel salts and sodium hypophosphite are dissolved in water solution and then the divalent Ni ions are reduced to the metallic form. The obtained resistive layers are characterized by a very low temperature coefficient of resistance (TCR), excellent hardness and very good resistance to corrosion.

In this project the authors elaborated a modification of the above mentioned procedure to obtain precise resistors characterized by low resistance in the range 0.2÷0.5 Ω, and excellent TCR coefficient at the level of 5 ppm/K. This new method called "multi-stage metallization" is a periodic process in which the basic chemical solution is replaced after every 1 hour, thanks to which the high purity solution is used during a metallization process. When using this procedure, a prediction of final values of resistance and TCR coefficient for the obtained resistive layers can also be assured.

K. Waczyński (PhD), E. Wróbel (PhD), W. Filipowski (PhD), *Investigation of the optical properties of dielectric layers of spin-on silicon glasses*

The deposition of spin-on glass silicon solutions on the Si wafer is one of the most commonly used techniques for the preparation of the solar cells emitter layers. One of the most critical points is the thickness of dielectric layers formed by the spin-on technique. This report presents the results of the experimental study of optical properties of the dielectric layers deposited on Si substrates, with a special emphasis on the thickness and refractive index of these layers. In our study an SE–400 Sentech Ellipsometer was used. On the basis of the performed experiments the following information was obtained:

- the spin-on technique enables the formation of dielectric layers of thickness $x_o = 68 \pm 5$ nm and refractive index $n = 1.4148 \pm 0.020$,
- the thickness and refractive index in the dielectric layer are strongly affected by the viscosity of the spun solution; however, no influence of the spinning rate was observed in the range 500÷6000 rpm,
- the quality of deposited layers strongly depends on the cleanliness of the laboratory room, working temperature, and relative humidity of the ambient air.

The obtained results will be used for further optimisation of spin-on-glasses technology for preparation of Si emitter layers for solar cells.

D. Komorowski (PhD), S. Pietraszek (PhD), *The Preliminary Study of the EGG and HR Examinations*

Electrogastrographic examination (EGG) can be considered as a noninvasive method for investigation of a stomach slow wave propagation. The EGG signal is non-invasively captured by appropriately placed electrodes on the surface of the stomach. In the project a method for synchronously recording and analyzing both the EGG and the heart rate signal (HR) has been developed. The HR signal is obtained by analyzing the electrocardiographic signal (ECG). The ECG signal is recorded by means of the same electrodes. A method of reconstruction the respiratory signal (RESPIRO) has also been applied. This way it is possible to examine mutual interaction between ECG, HR and RESPIRO signals, respectively. Preliminary results of a comparison between the EGG and the RESPIRO signals have been obtained using two different methods, first, by classical pass-band filtering, secondly, by estimation of the baseline drift.

The standard surface EGG signals were captured by means of disposable electrodes placed on the patient's stomach surface. During the signal registration process standard electrodes were applied configured according to the standard, including four signal electrodes (E1..E4), the reference electrode (Ref) and the ground electrode (Gnd).The signals which are available on the stomach surface include not only the EGG signal but also ECG signals and signals connected with respiratory movements. Both useful components of the EGG and RESPIRO signals are localized in the same range of frequency. The signals were recorded within the 0.015Hz - 50Hz frequency range. In popular commercial systems for capturing the EGG, the signals are usually obtained by means of the method based on classical pass-band filtration. The filtration typically is made by using analog filters placed after a preamplifier stage. The typical cutoff frequencies are 0.015Hz and 0.15Hz. The recording of additional signals requires other devices, so that synchronous signals analysis becomes difficult. The developed methods of capturing and analyzing signals obtained from the stomach surface allow to separate the components of the EGG, HR and RESPIRO signals. In this way simultaneous analysis of the EGG and the HR obtained from the ECG signals is possible.